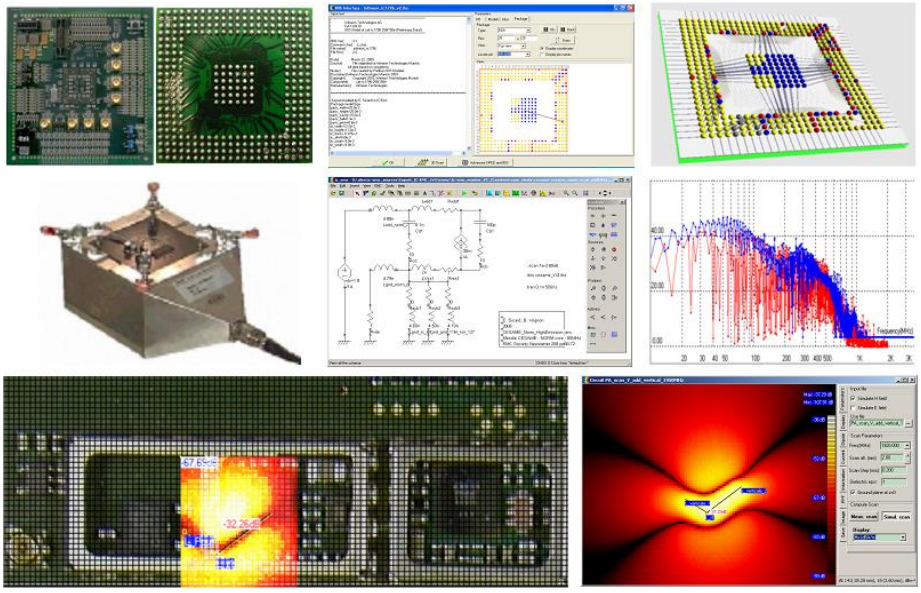
IC-EMC

User's Manual

Version 2.9



www.ic-emc.org

Alexandre BOYER

Etienne SICARD

INSA Toulouse, France

September 2022

INSA TOULOUSE, University of Toulouse France, 2022
INSA 2005-2018
135 Av de Rangueil
31077 Toulouse France

Download

- The software IC-EMC can be downloaded from www.ic-emc.org

About the Authors

Etienne SICARD was born in Paris, France, June 1961. He received the B.S degree in 1984 and the PhD in Electrical Engineering from the University of Toulouse, in 1987, in the laboratory LAAS of Toulouse. He was granted a Monbusho scholarship and stayed 18 months at Osaka University, Japan (1988-1989). Previously a professor of electronics in the Department of Physics, University of Balearic Islands, Spain (1990), Etienne SICARD is currently a professor at INSA of Toulouse, France, Department of Electrical and Computer Engineering. He is an associated researcher at IRIT, the Toulouse Institute of Computer Science Research. His research interests include several aspects of integrated circuits (ICs) for improved electromagnetic compatibility (EMC), and speech processing applied to speech therapy.

Email: etienne.sicard@insa-toulouse.fr

Web page: http://intranet-gei.insa-toulouse.fr/~sicard/

Alexandre Boyer was born in Annemasse, France, in 1981. He obtained Master degree in electrical engineering in 2004 and a PhD in Electronics from the Institut Nationale des Sciences Appliquées (INSA) in Toulouse, France, in 2004. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at INSA, Toulouse. He is also a member of the LAAS-CNRS research centre dedicated to the analysis of complex systems. His current research interests include EMC modeling at IC and PCB level. He has more than 10 years' experience in research into and training on the EMC of ICs.

Email: alexandre.boyer@insa-toulouse.fr

Web page: www.alexandre-boyer.fr

Table of Contents

I. Introduction

This manual document describes the tool IC-EMC (acronym for Integrated Circuit Electromagnetic Compatibility) which aims at simulating parasitic emission and susceptibility of integrated circuits and eases the comparison with measurements. The tool uses the simulators WinSpice, Ngspice and LTSPICE® for SPICE simulation. The software can be downloaded on www.ic-emc.org.

IC-EMC is a free simulation software entirely dedicated to the EMC of ICs issues. IC-EMC is not geared to full-chip simulation coupled with a 3D electromagnetic solver and is not intended to address complex EM problems. It aims at developing simple models of ICs and its surrounding environment (IC package, PCB traces, cables) for simulation of emission, susceptibility and signal integrity. Its purpose is twofold:

- help the user to develop EMC models rapidly for an efficient evaluation of EMC performances
- illustrate EMC issues related to ICs for educational purpose of basic notions and modelling techniques related to EMC

To obtain more accuracy or to address more complex problems, we advise you to use the professional CAD tools available in your university, lab or company

This manual is organized as follows:

- The second section (Getting started) presents an overview of the software and describe how to install and launch it
- The third section (Working with IC-EMC) shows the different possibilities of the software through several practical examples
- The fourth section (Description of the menu) describes the different menus of the software
- The fifth section (Description of the symbols) lists all the symbols proposed by the software to build electrical schematic diagram
- The sixth section (Input/output file format) describes the different exchange files used by the software

The authors have dedicated around ten years to build the technical contents of this manual and software, and tried their best to improve the IC-EMC tool, trying to keep the usage simple. As the tool is in constant evolution, we encourage the reader to download the updated version of IC-EMC form the web page and we would appreciate feedback and comments.

Acknowledgements

We wish to warmly acknowledge all our former PhD students who developed numerous case studies presented in this manual: Bertrand Vrignon, Enrique Lamoureux, Cécile Labussière, Samuel Akue Boulingui, Céline Dupoux, Mickael Deobarro, Amadou Cisse Ndoye, Bihong Li, He Huang, Laurent Guibert, Veljko Tomasevic and Chaimae Ghfiri. We would also like to thank Sonia Ben Dhia and Sebastien Serpaud for their positive support and constructive remarks about IC-EMC, together with all our colleagues in the area of electromagnetic compatibility of integrated circuits who inspired us through fruitful discussions and collaborative research.

Our thanks too to all the research project leaders who co-funded our research, contributed to the development and the improvement of IC-EMC (MEDEA, EPEA, SEISME, ANR, IRT Saint-Exupéry and European program Erasmus+ Knowledge Alliance - MicroElectronics Cloud Alliance).

Toulouse, September 8, 2022

Alexandre Boyer, Etienne Sicard

II. Getting started with IC-EMC

IC-EMC is a simulation software entirely dedicated to the EMC of ICs issues. It works only with Windows Vista and Windows 7 or 10. IC-EMC is a schematic editor interfaced with three free SPICE simulators: WinSPICE, Ngspice and LTSPICE. By exploiting simulation results provided by these simulators, IC-EMC proposes a set of post-processing tools to extract relevant EMC information. The section aims at presenting an overview of the software and how to install and launch it.

II.1 Overview of the software

The tool IC-EMC is able to perform comparisons between measurements and simulation of conducted, radiated emission, near-field emission, S and Z parameters, immunity and signal integrity, as illustrated in Figure 2- 1. Moreover, it includes also different tools to build models of IC package, PCB traces and cables.

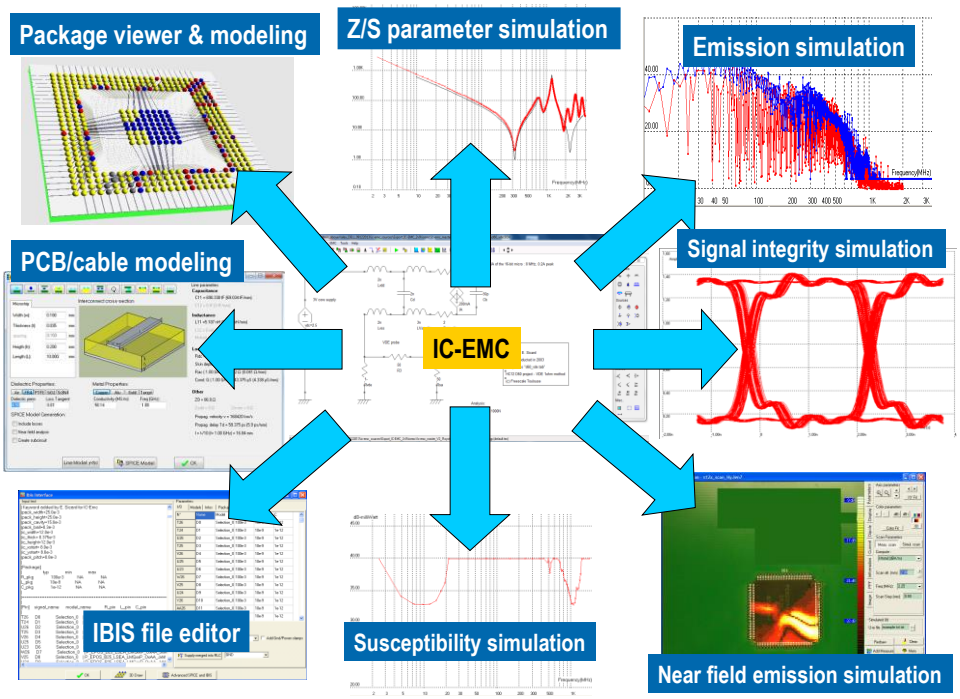


Figure 2- 1: Main features of IC-EMC

The main commands of IC-EMC are shown in Figure 2- 2. From left to right, the Spice Simulation icon translates the schematic diagram into a SPICE compatible text file, the next icons give access to the emission spectrum window, the impedance vs. frequency, the immunity simulation screen, and the near-field simulation screen.

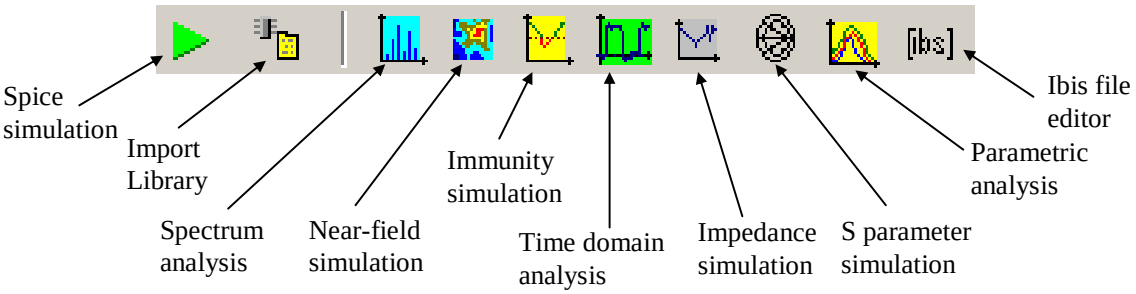


Figure 2- 2: Main commands proposed by -EMC

Figure 2- 3 describes the general simulation flow with IC-EMC. The process starts with the edition of the circuit schematic. Component models are provided by IC-EMC or external libraries. The netlist file generated by IC-EMC serves as input file for the SPICE simulator (WinSPICE, Ngspice or LTSPICE). At the end of the simulation, SPICE simulation results are exploited by IC-EMC post-processing tools. Different measurement file formats can be imported to compare simulation and measurement results and tune simulation models.

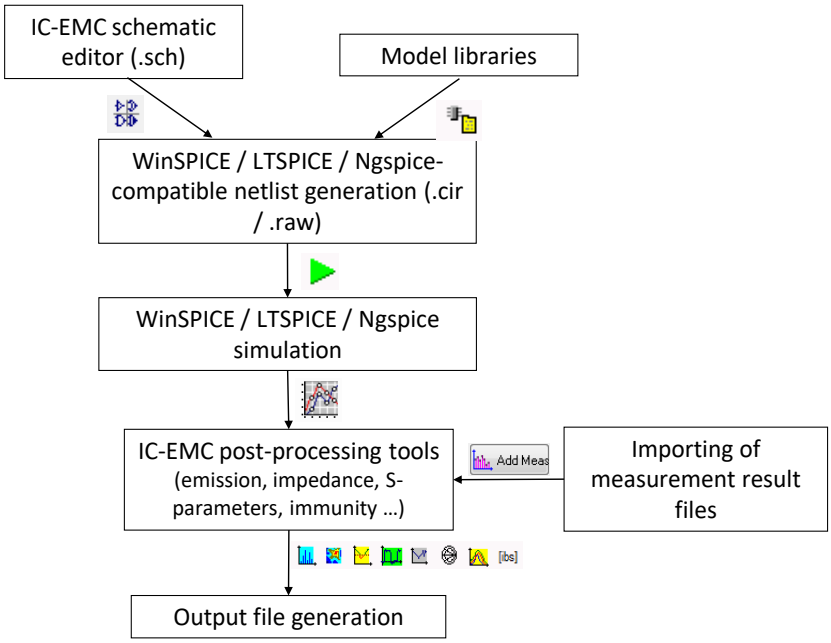


Figure 2- 3: General simulation flow with IC-EMC

II.2 Installing and running IC-EMC

The following paragraphs detail the different steps for installing, running and exiting the software.

II.2.1 Download the Schematic Editor

The software can be downloaded from www.ic-emc.org. The zip file contains an executable file (icemc.exe) and folders containing libraries and examples.

After downloading and unzipping the IC-EMC software package, a main directory called “IC-EMC-2v9” is displayed. This directory contains a list of subdirectories organised as shown in Figure 2- 4.

It contains the IC-EMC executable file (ic_emc.exe) and a further collection of subdirectories. Some of them contain examples and case studies, while others contain component libraries. Their content is briefly described in Table 2- 1.

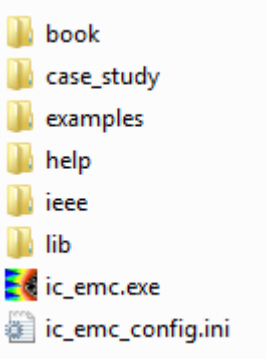


Figure 2- 4: Organisation of the main directory IC-EMC-2V9

Subdirectory name	Contents
book	The subdirectory contains the schematic diagrams and measurement results presented in the book: A. Boyer, E. Sicard, "Basis of Electromagnetic Compatibility of Integrated Circuits", Collection Pour l'Ingénieur, Presses Universitaires du Midi, 2017.
case_study	The subdirectory contains schematic diagrams and measurement results related to several case studies described on the website www.ic-emc.org
examples	The subdirectory contains various schematic diagram related to basic notions of EMC, emission, near-field, susceptibility...
help	HTML pages of online help
ieee	Symbol library used by IC-EMC (*.sym). Some are available from the palette (see 11.2.7), while others can be downloaded by clicking on “Insert → User Symbol (.SYM)”.
lib	.tec file and default non-linear device SPICE library (.lib) (e.g. a diode, BJT, CMOS transistor, non-linear capacitor, switch)

Table 2- 1: Content of the subdirectories of the main directory IC-EMC-2v9

II.2.2 Download WinSPICE

The WinSPICE analogue simulation tool may be downloaded from www.winspice.co.uk. Click on the  icon to run the WinSPICE solver wspice3.exe. It is necessary to define in IC-EMC the access path of the solver wspice3 (see II.2.6).

II.2.3 Download LTSPICE

The LTSPICE free simulation tool (LTSPICE XVII) may be downloaded from https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html.

Click on the icon to run the LTSPICE XVII solver XVIIx64.exe. It is necessary to define in IC-EMC the access path of the solver XVIIx64 (see II.2.6).

II.2.4 Download Ngspice

The Ngspice free simulation tool may be downloaded from http://ngspice.sourceforge.net/.

Click on the icon to run the solver ngspice.exe. It is necessary to define in IC-EMC the access path of the solver Ngspice (see II.2.6).

II.2.5 Initial Screen

To launch IC-EMC, double-click on executable file ic_emc.exe in the main directory of IC-EMC. The following figure presents the interface when the software opens. The editor contains a palette of symbols (Window "Symbols" situated on the right of the screen) and some basic editing icons to build the schematic diagram of the circuit and control the main EMC screens.

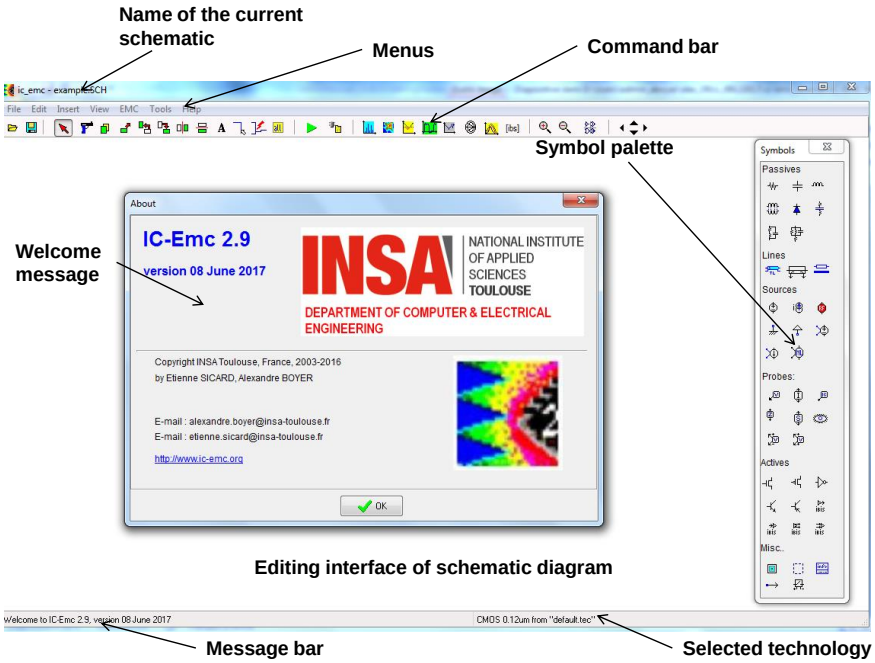


Figure 2- 5: IC-EMC user interface

The symbol palette gives access to the most common elements of electrical schematics, such as passive devices, voltage and current sources, transmission lines and interconnects, measurement probes for voltage, current, impedance, power, S-parameters etc., in addition to diodes, MOS devices, bipolar junction transistors and input/output buffer models extracted

from an IBIS file. The components of the symbol palette are described in **Erreur ! Source du renvoi introuvable.**. The palette is visible as soon as IC-EMC is run. If the palette is closed accidentally, it can be reopened by clicking on "View > Symbol Palette" or clicking on the icon in the command bar.

All the components placed on schematic diagrams are described in a .sym file, which describes both the graphical aspect of the component in the schematic and the SPICE model of the component. Not all the components supported by IC-EMC are in the symbol palette. IC-EMC proposes additional components that can be inserted in the schematic through the Insert / User Symbol (.SYM) command. They can be either constructed by the user as a SPICE subcircuit (using command "File > Generate SPICE Subcircuit"), or found in the list of symbols in the "ieee" subdirectory. More information about the symbols contained in the system/ieee directory can be found on the IC-EMC companion website.

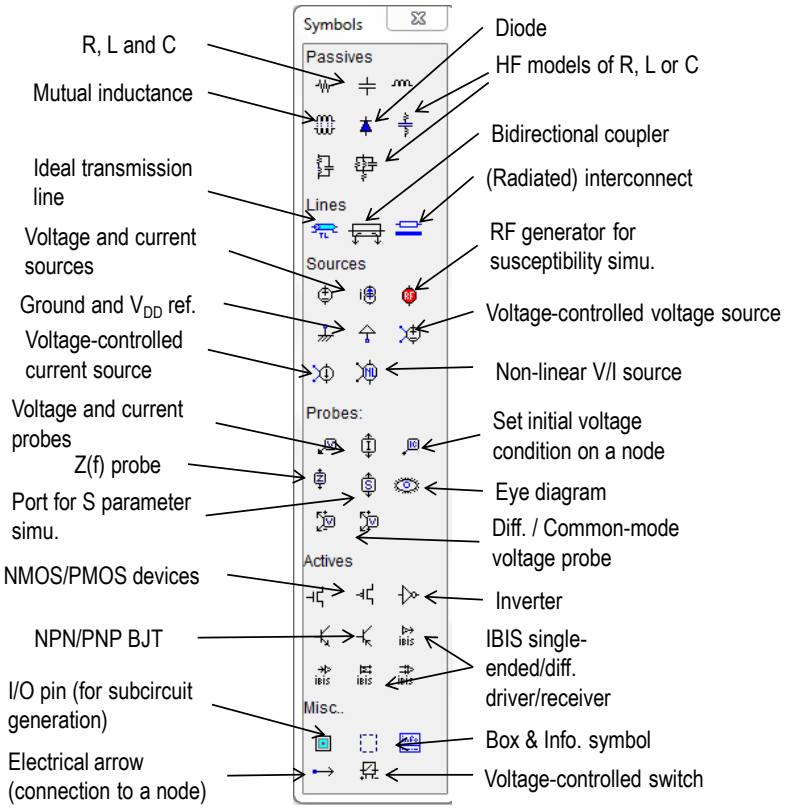


Figure 2- 6: Symbol palette

The main commands for EMC and post-processing can be found in the EMC menu or the command bar, as shown in Figure 2- 7. After editing the schematic and setting the simulation parameters, click on the 'Generate SPICE netlist' button to translate the schematic diagram into a SPICE-compatible text file. This step is necessary before any new SPICE simulation or post-processing of results. The following icons give access to the main post-processing tools (e.g. emission window, near-field simulation, immunity simulation, Z- and S-parameters etc.).

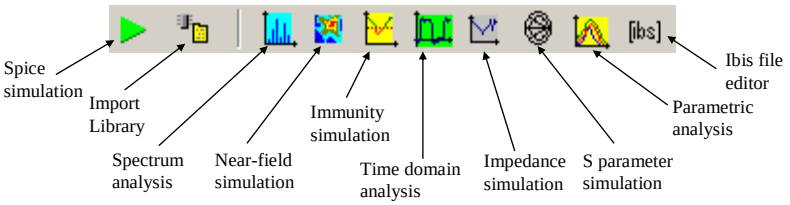


Figure 2- 7: Main simulation commands

II.2.6 Configure simulator options

Before launching SPICE simulations, it is necessary to define the access path of the simulators (WinSPICE, Ngspice and LTSPICE) and the launching options. It can be configured by clicking on the command menu "File > Simulator > Configurations". The following window opens.

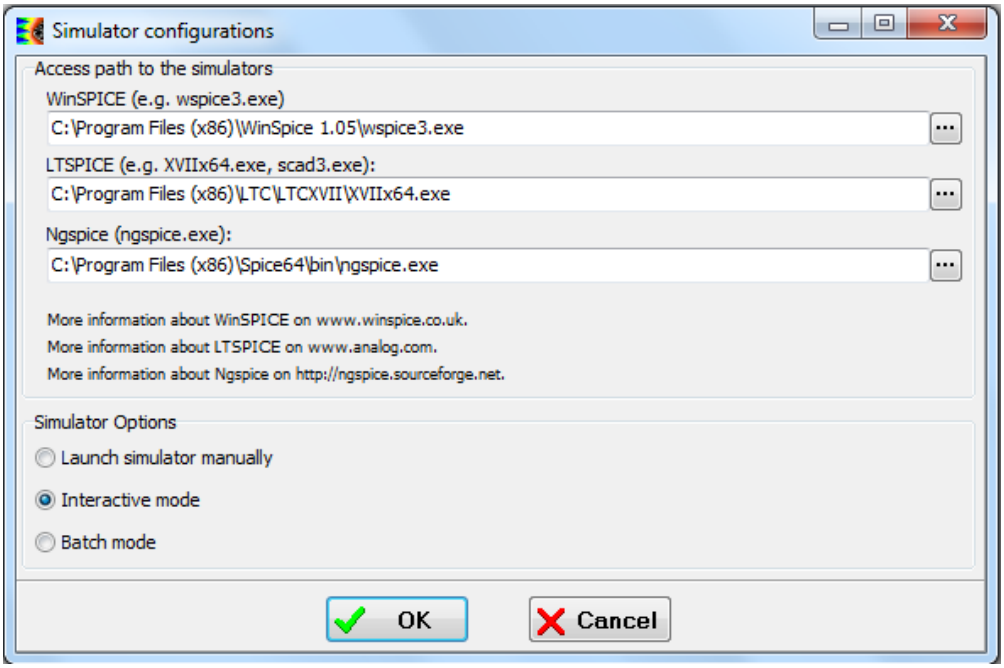


Figure 2- 8: Simulator configurations (File > Simulator > Configurations")

Set the access path of WinSPICE, LTSPICE and Ngspice simulator executable files in the fields "WinSPICE", "LTSPICE" and "Ngspice" by clicking on the button ... This operation has to be done manually each time the user reinstalls SPICE simulators and their installation directories. In the lower part of the screen, three simulation options are proposed:

- Launch simulator manually: when the user generates SPICE netlist , he has to launch the simulator, opens the circuit netlist (.cir file) and launch the simulation
- Interactive mode: when the user generates SPICE netlist , the simulator is automatically launched and remains opened at the end of the simulation to analyze the result
- Batch mode: when the user generates SPICE netlist , the simulator is automatically launched but is closed directly at the end of the simulation

II.3 Using IC-EMC

II.3.1 Create my first model

As first simple example, we consider a resistive voltage divider excited by a sine waveform signal at its input. The divider is made of two resistance of 1 KΩ. The amplitude of the signal is 1 V and its frequency is set to 100 MHz. The simulation aims at predicting the transient waveform of the voltage at the output of the resistive divider.

Double-click on executable file ic_emc.exe to launch the software. if it is already opened, click on the command "File > New" or "CTRL+N" to create a new schematic diagram.

Pick two resistor symbols in the Symbol palette, drag and place them on the schematic. These symbols are called R1 and R2 by default. Their default resistance is 50 Ω. Click on the icon to rotate to the right the resistor R2. The result is shown in Figure 2- 9. To change the properties of the symbols (name and resistance), double-click on the symbol. The window shown in Figure 2- 10 opens. Change the resistance value of both resistors to 1 K in the field "Value". To change the name of a symbol, write the new name in the field "User name". To validate the change, click on the button OK or type "Enter" key.

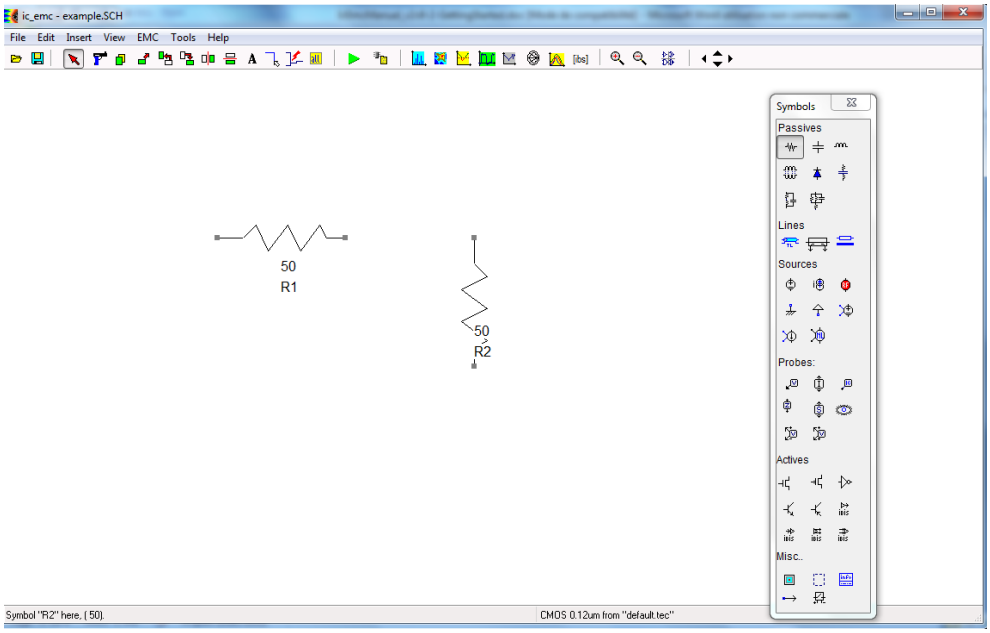


Figure 2- 9: Place two symbols of resistor on a schematic diagram

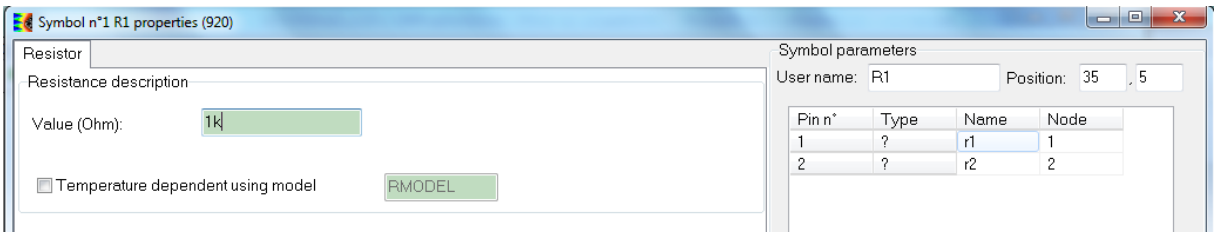


Figure 2- 10: Change the resistance value of a resistor symbol

Then, pick the voltage source symbol in the Symbol palette and place it on the schematic diagram on the left of R1 (Figure 2- 11).

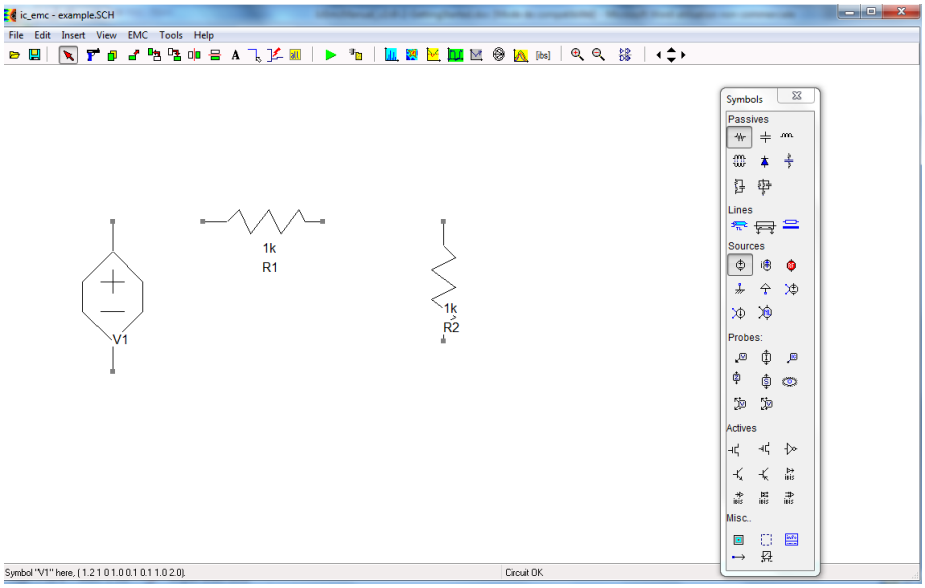


Figure 2- 11: Place one voltage source symbol on a schematic diagram

Double-click on the voltage source symbol to edit its properties. Click on the tab "Sine Parameters" to set a sine waveform generator. The following parameters are proposed:

- VO: offset voltage (V)
- VA: amplitude of the sine waveform (V)
- Freq: frequency (MHz)
- TD: delay (ns)
- Theta: damping factor (1/s)

Use the parameters shown in Figure 2- 12 and click on the button OK

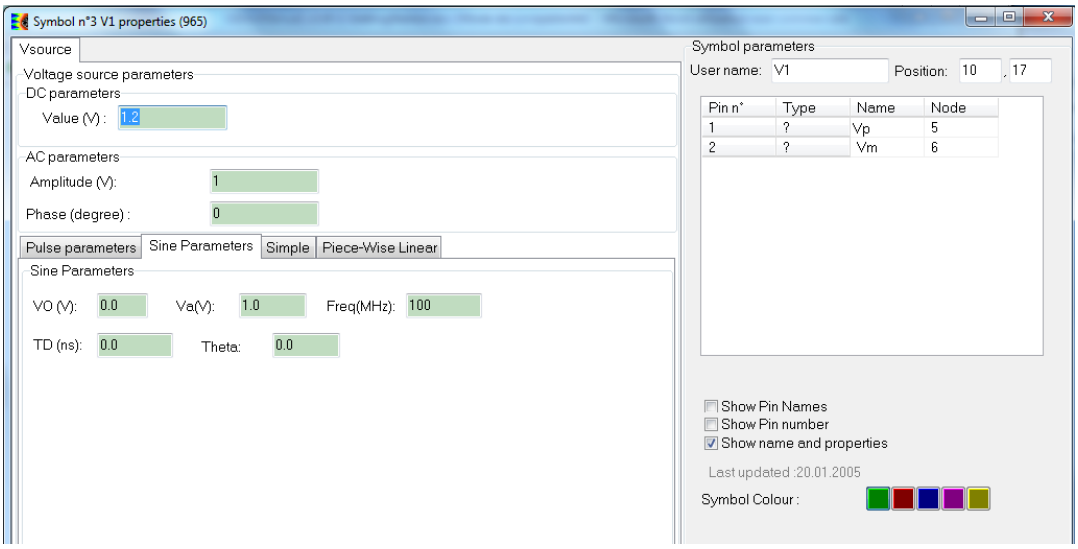


Figure 2- 12: Edit the properties of a voltage source

All the electrical components of the circuit have been placed. Now, they have to be interconnected. Interconnections between symbol's nodes are ensured by wires. To add

wire, click on the icon "Line" or on the menu "Edit > Line". Line edition mode is activated and wires are created between two points selected on the schematic with the left button of the mouse. The line edition mode is deactivated by clicking on the icon "Select" or hitting the ESC key. Alternatively, line edition mode can be activated by clicking on the schematic with the left button of the mouse. Place wire between the different terminals of the symbols. Terminals are highlighted by square symbol . The result is shown in Figure 2- 13. Before simulation, it is necessary to indicate the voltages and currents that we want to observe by placing voltage and current probes on the schematic diagram. Voltage probes are connected on one node of the diagram while current probe are placed within one circuit branch. In this example, place two voltage probes: one at the divider input (between V1 and R1), the other at the divider output (between R1 and R2).

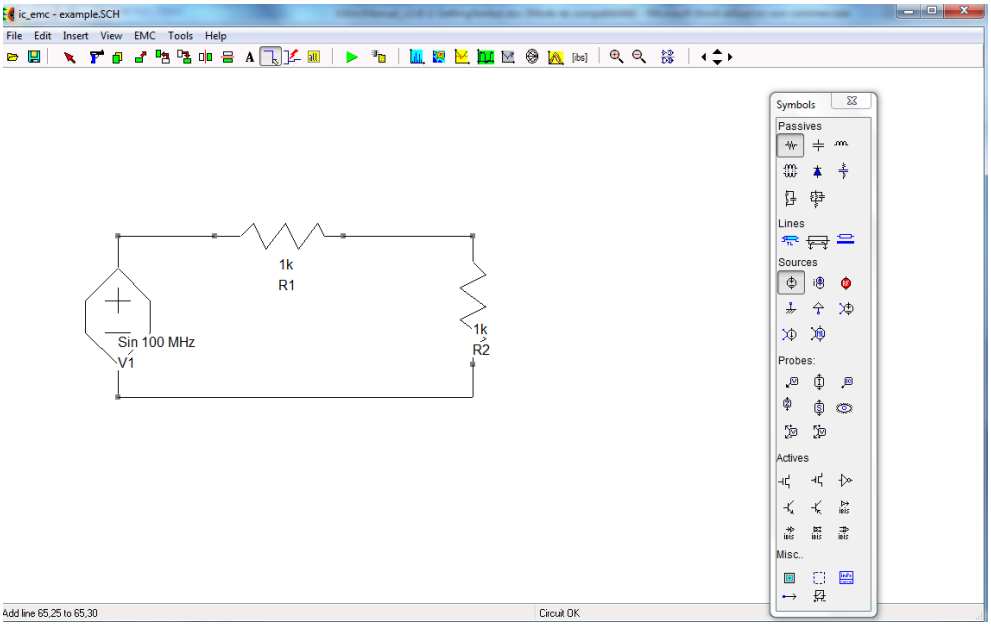


Figure 2- 13: Place wire to interconnect the different symbols of the schematic diagram

The schematic diagram is nearly terminated, but an important element has been forgotten. In any SPICE netlist, a '0' or reference node has to be defined. Forgotting such reference node will result in simulator error. Place the symbol "Ground" on the schematic, between V1 and R2. The final schematic diagram is shown in Figure 2- 14.

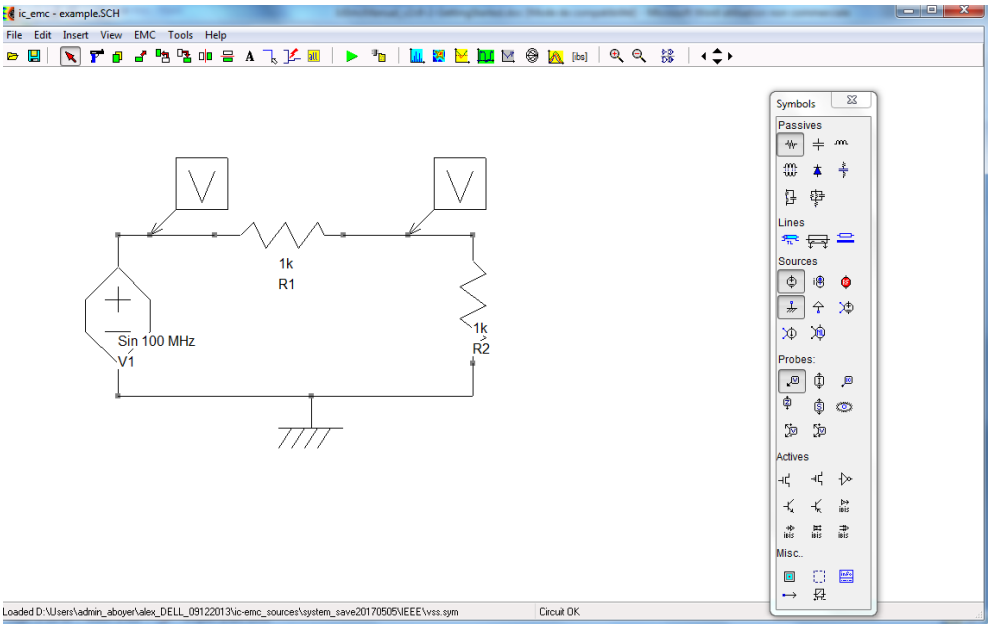


Figure 2- 14: Place voltage probes and the ground symbol

Before launching the SPICE simulation, IC-EMC converts the schematic diagram into a netlist (file .cir) compatible with WinSPICE, Ngspice or LTSPICE. This netlist describes the circuit in components whose terminals are referenced by number. Each number indicates a node of the schematic diagram. All the terminal with the same node number are connected electrically. To see the number of the different nodes forming the schematic diagram, click on the icon  or on the menu "View > View Electrical Net" (Figure 2- 15). Voltage probes have been placed on nodes 1 and 2. This view can be convenient to verify electrical connections between the symbols during debug.

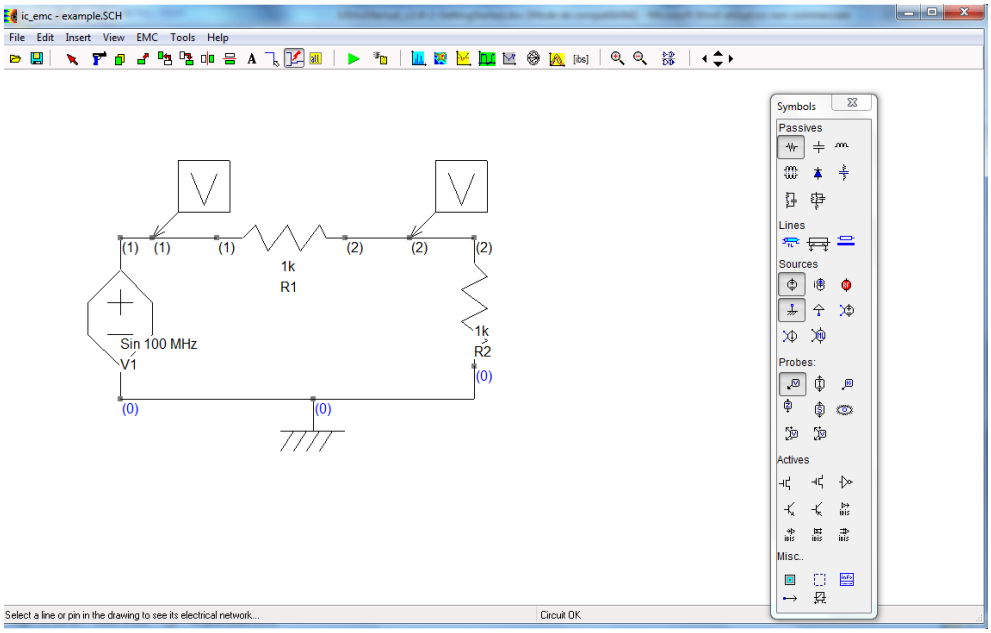


Figure 2- 15: View the nodes of the schematic diagram (icon )

II.3.2 Save the schematic diagram

Before launching any simulation, it is extremely important to save the schematic in a known directory. Click on "File > Save as" or on the icon or CTRL+S to save the schematic diagram. They are saved in .sch file. Save it as Voltage_Divider.sch. The final version of this schematic diagram is available in the directory "\examples\basic\FFT".

II.3.3 Prepare the analysis

SPICE simulator proposes different analyses (DC, AC, TRAN...). The analysis is defined and configured by a analysis command line added to the schematic. Here, we want to set a transient simulation. The most convenient way to set simulation parameters for beginners is to click on "Insert > Insert analysis line". The following window open to set up the SPICE analysis. Select the tab "Transient analysis" and set:

- Stop time: 100 ns
- Step time: 0.1 ns

The SPICE analysis command line appears at the bottom of the window and is updated each time the analysis parameters are changed. The format of the analysis line is also shown. Finally, click on the button "Insert" and click "Close". The analysis line is automatically inserted on the schematic diagram, as shown in Figure 2- 17. Alternatively, the analysis line can be directly added on the schematic by clicking on the icon and type the command line ".tran 0.1n 100n".

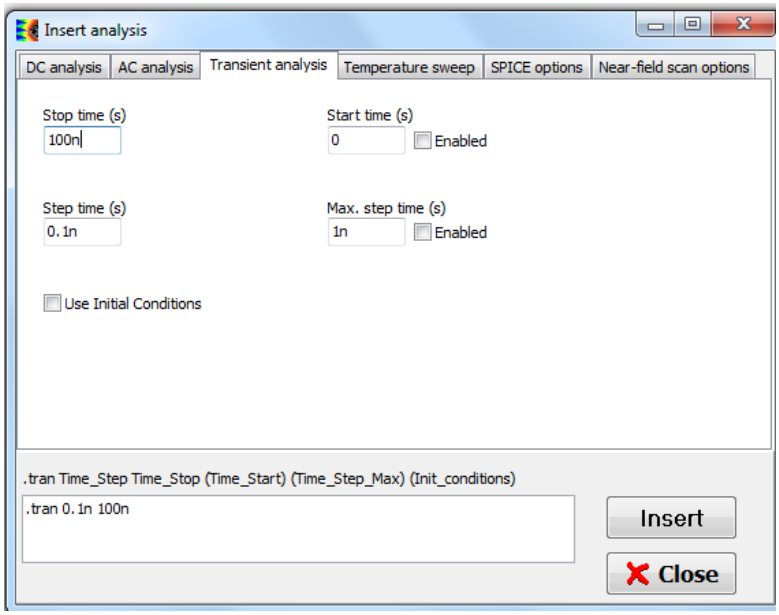


Figure 2- 16: Define the SPICE analysis

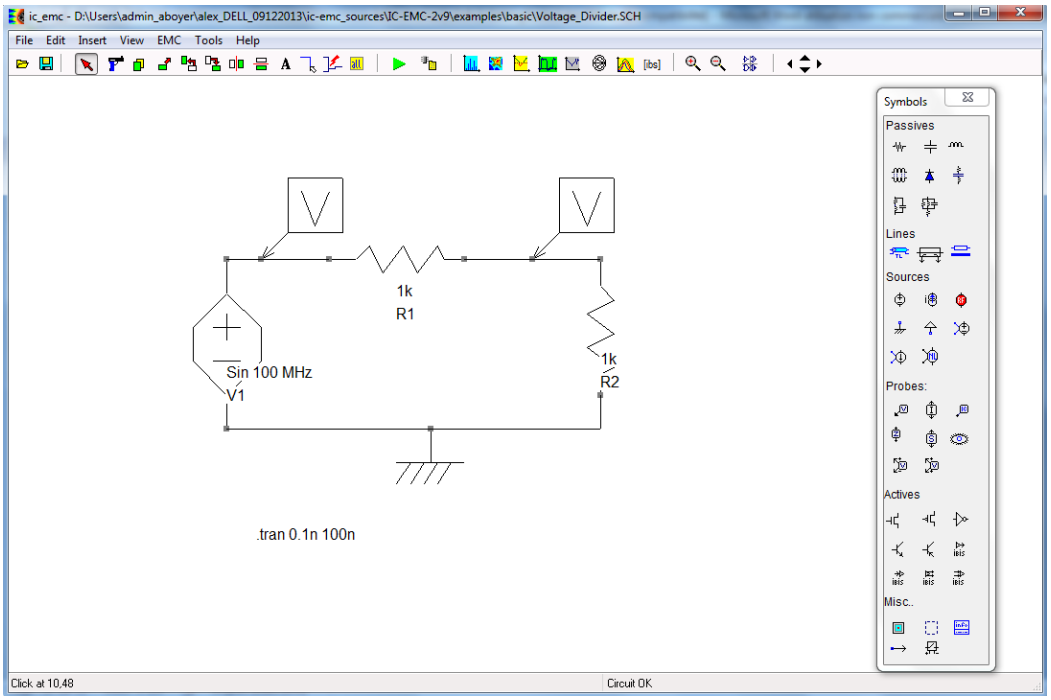


Figure 2- 17: Insert the SPICE analysis line on the schematic diagram

II.3.4 Launch my first simulation

Before launching your first simulation, you should ensure that the access paths of the simulators have been defined as explained in part II.2.5. Two SPICE simulators are supported by IC-EMC: WinSPICE, Ngspice and LTSPICE. To select a simulator, click on the menu "File > Simulator" and select "WinSPICE", "Ngspice" or "LTSPICE". In this example, WinSPICE will be used. Click on the menu "File > Simulator > Configurations" and select the option "Interactive mode": the simulator will be launched automatically when the netlist will be generated.

Click on the button  or on the menu "EMC > Generate SPICE file" or hit CTRL+G to launch the simulation. Actually, this command is twofold:

- the electrical schematic diagram is converted in a netlist, saved in a .cir file. The netlist file has the same name than the schematic file (Voltage_Divider.cir). The window shown in Figure 2-18 appears when the netlist file is generated to verify the content of the netlist. Click on the button "OK" to close this window.
- in "File > Simulator > Configurations", if the options "Interactive mode" or "Batch mode" have been selected, then the SPICE simulation is automatically launched. If the option "Launch simulator manually" is selected, then the user has to launch the simulator and select the .cir file.

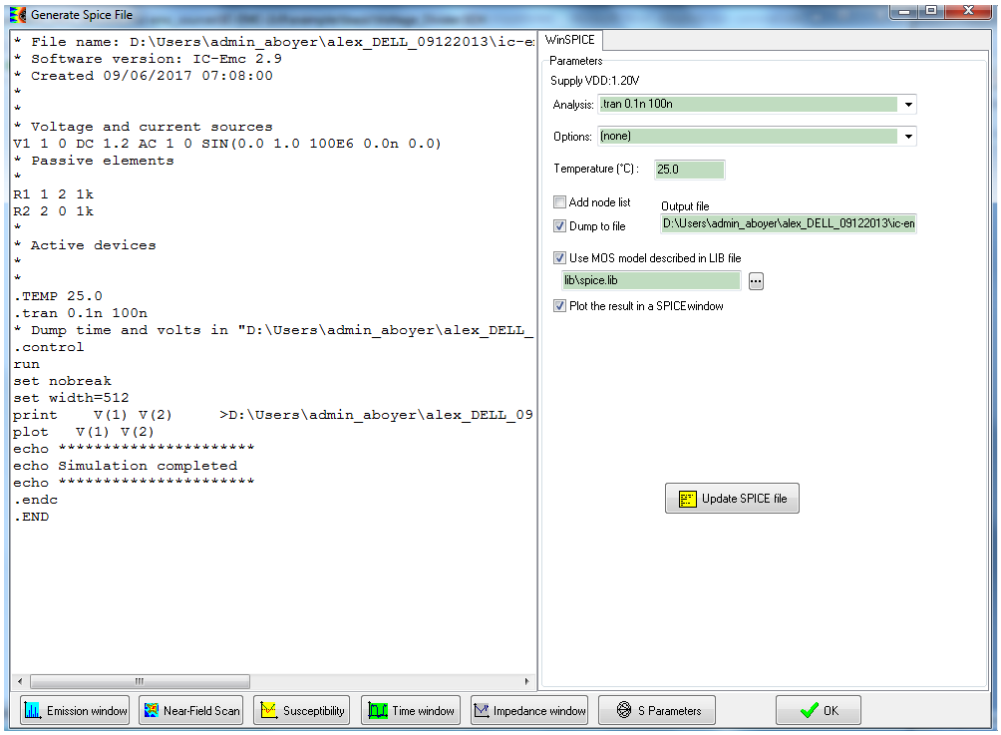


Figure 2- 18: Generation of the netlist file

SPICE simulation is launched automatically and the WinSPICE interface opens. At the end of the simulation, the message "Simulation Completed" is displayed on the WinSPICE interface and the simulation result is displayed (Figure 2- 19). IC-EMC proposes tools to analyze simulation results, as described in the next part and the next chapter of this manual.

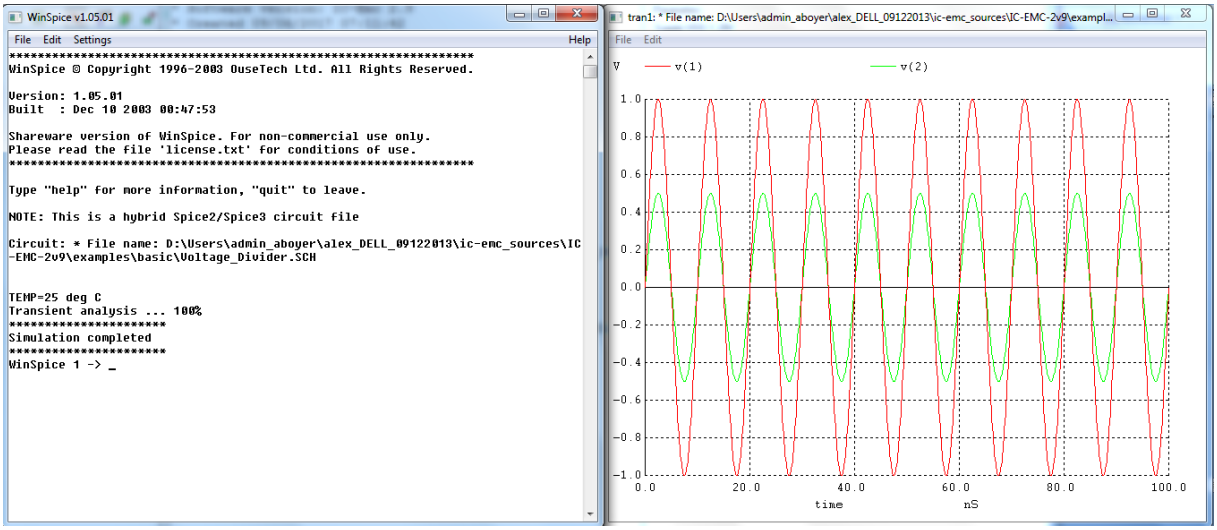


Figure 2- 19: WinSPICE simulation launching and result

II.3.5 Analysis result

First, the transient waveforms of input and output signals are analyzed. Open the "Voltage vs. Time" window by clicking on the button  or on the menu "EMC > Voltage vs. Time", presented in Figure 2- 20. The signals associated to the voltage probes added on the

schematic diagram appears on the list "Signal" in the top-right part of the window. Select both signals (v(1) and v(2)) and click on the button "Add Simu" to plot them.

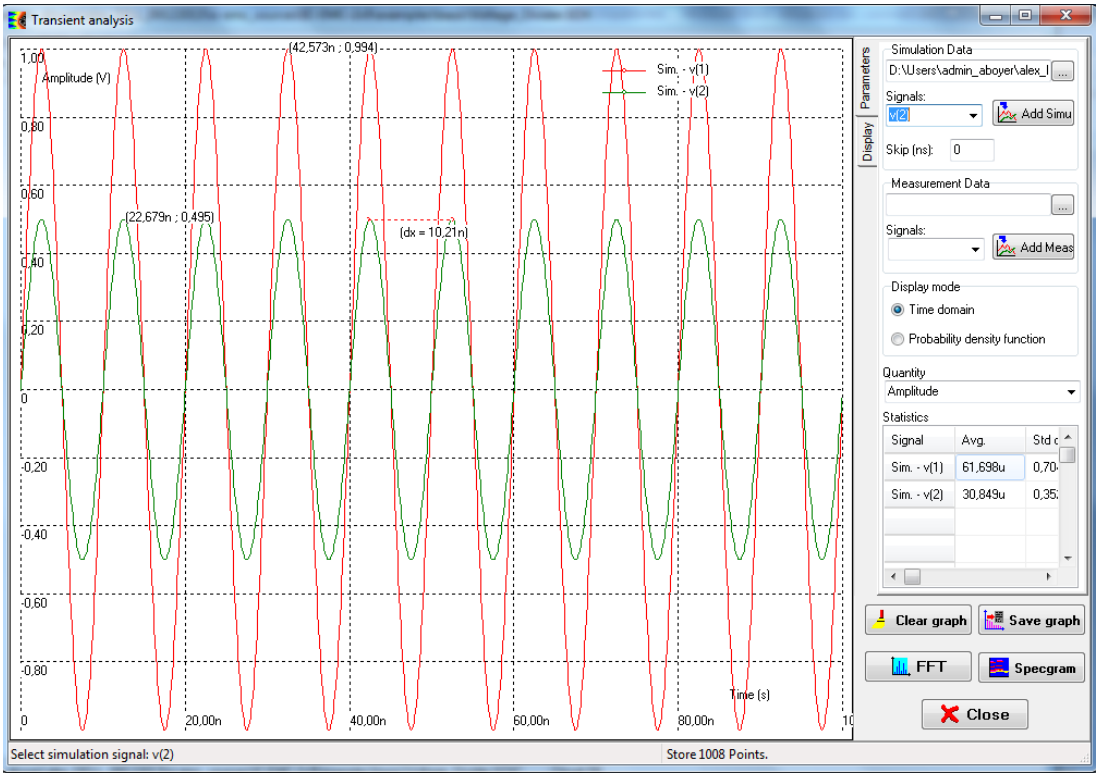


Figure 2- 20: Time -domain analysis with IC-EMC ("EMC > Voltage vs. Time")

In the tab "Display", different options are proposed to change the axes settings. Amplitude and period characteristics can be extracted by clicking directly on the graph. More indicators are available in this tool. They will be described in the next chapters. A practical example is shown in III.6. Close the window by clicking on the button "Close".

Then, the spectrum of the input signal is analyzed. Click on the icon or on the menu "EMC > Emission vs. Frequency". The window shown in Figure 2- 21 opens, showing the spectrum of the input and output signals of the voltage divider. The spectrum is computed by Fast Fourier Transform (FFT). The number of points can be changed to adjust the resolution by clicking on the list "Resolution" in the tab "FFT Parameters". Select 4096 points and a Blackman window. In the tab "Display", click on the button in the tab "Display" to set a logarithmic scale on Y axis. The voltages are expressed in dBµV, which is typical in conducted emission measurement.

The FFT result presents a large peak centered at 100 MHz. Its amplitude is equal to 120 dBµV, i.e. 1 V. This result is consistent with the sine wave nature of the signal. Click on the button "Close" to close this window.

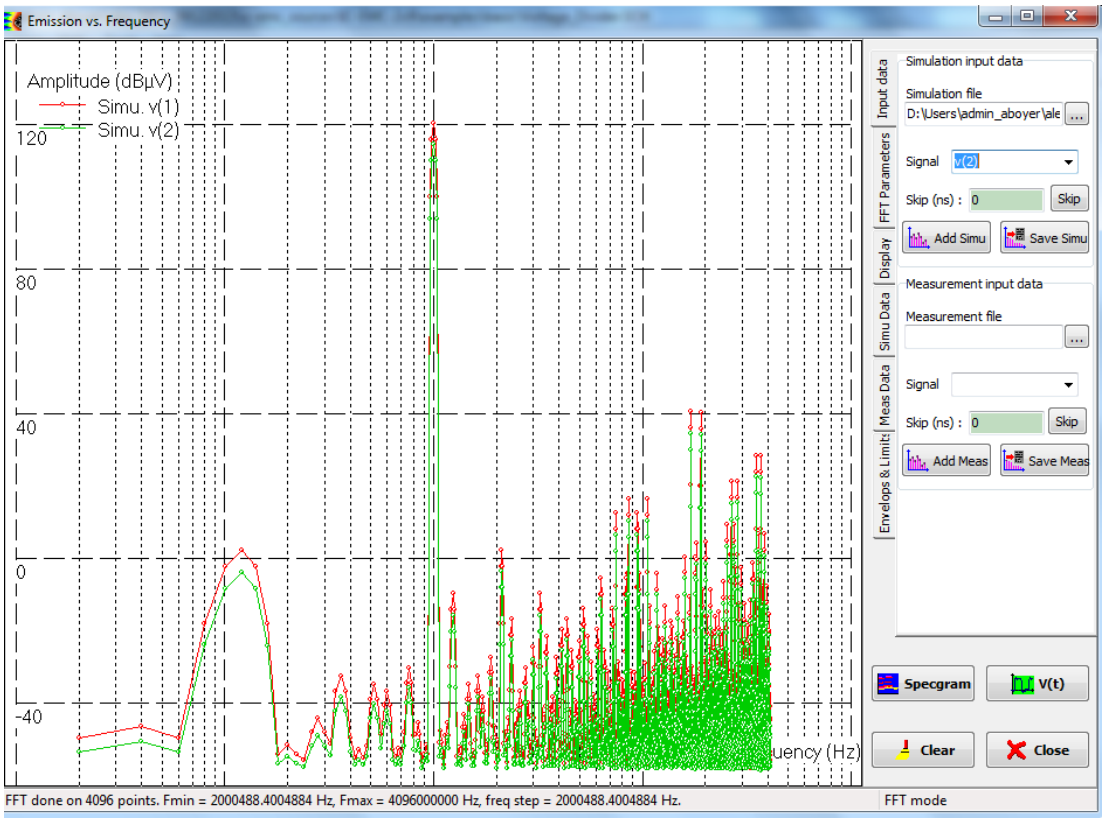


Figure 2- 21: Frequency -domain analysis with IC-EMC ("EMC > Emission vs. Frequency")

II.3.6 Close IC-EMC

Before leaving IC-EMC, save your schematic diagram by clicking on the icon or click on the menu "File > Save". Click "File > Exit IC-EMC" or hit CTRL+Q to close the software.

III. Working with IC-EMC

This part provides straightforward examples of how to use IC-EMC to create simple model of a circuit and perform the main analysis proposed by IC-EMC:

- simulation of electromagnetic emission based on the transient response of voltage or current
- simulation of impedance and S parameters of passive or active devices, PCB traces, cables...
- simulation of the conducted immunity of IC to harmonic disturbance
- analysis of IBIS file and extraction of equivalent models of I/O buffers
- analysis of transient signals (timing characteristics, statistical properties, short-term FFT)
- simulation of signal integrity and eye diagram plot
- simulation of near-field emission based on thin-wire approximation
- modelling of various type of interconnects (PCB traces, cables, IC package, power-ground plane pair)
- estimation of IC emission model

IC-EMC is also able to import measurement files to compare simulation with measurement results.

III.1 Simulation of the conducted emission of a microcontroller

This example presents the flow to simulate the conducted emission of a microcontroller, using a simplified microcontroller model. Simulated conducted emission measurements are related to the IEC 61967-4 standard's 1/150 Ω method [IEC61-4].

III.1.1 Open the example

Open file "examples\emission\mpc\mpc_vde.sch" (Figure 3- 1). The model includes a description of the microcontroller based on a set of RLC elements and a current source, according to the IEC62433-2 ICEM-CE model format [ICEM]. ICEM is an IEC standard dedicated to emission modelling. Moreover, resistances R_{VDE}, R_{49} and R_{SA} are added as an equivalent model of the current measurement probe defined by the IEC 61967-4 standard, also known as 1 Ω method. The meaning of the components forming the circuit model is given in Table 3- 1.

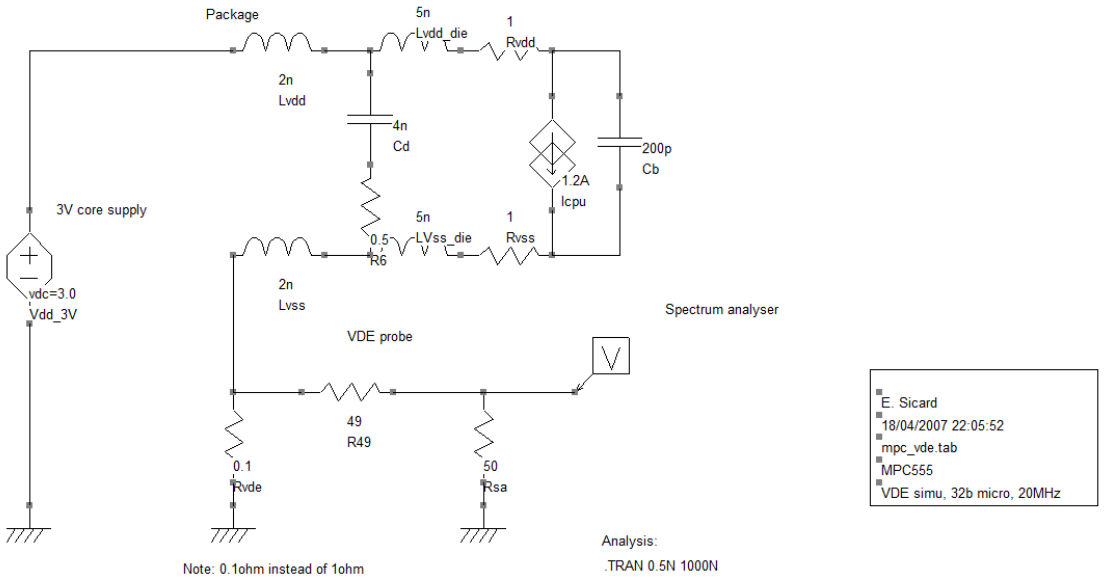


Figure 3- 1: The ICEM model of a 32-bit microcontroller (examples\emission\mpc\mpc_vde.sch)

Parameters	Description	Remarks
Ib	Current source Unit: Ampere Description: piece-wise-linear	*The Ib current is described as a periodic triangle (1.2 A max)*
Cd	Decoupling capacitance Unit: Farad Description: discrete C	*Cd is 4 nF, which is quite high due to on-chip added capacitance*
Lvdd_die, Lvss_die	Series internal inductance Unit: Henry Description: discrete L	*The series inductance is tuned to 5 nH, which provokes a resonance effect with Cb around 300 MHz.*
Rvdd_die, Rvss_die	Series internal resistance Unit: Ohm Description: discrete R	*Around 1 ohm series resistance due to long on-chip metal traces*
Cb	Block decoupling capacitance Unit: Farad Description: discrete C	*Local block capacitance, around 200 pF.*
Rvde, R49, Rsa	Current probe, matching resistors, and input impedance of spectrum analyser respectively Unit: Ohm Description: discrete R	*The current probe resistor is usually equal to 1 ohm. To reduce voltage drops across this resistor, it has been replaced by 0.1 ohm.*

Table 3- 1: Details on the circuit model's electrical components (examples\emission\mpc\mpc_vde.sch)

Lvdd and *Lvss* concern the package, and account for the series equivalent inductance from the IC die to the physical supply source and the VDE probe. Notice that the series resistance is 0.1 Ω instead of 1 Ω due to the high current flowing inside the IC. Placing a 1 Ω series resistance would dissipate nearly 1 W and induce a voltage drop of around 1 V, which is unacceptable. The voltage measured by spectrum analyser V_{SA} across the 0.1 Ω resistor is related to IC current I_{gnd} returning to the ground through the resistance by the following theoretical relation (if PCB and passive device interferences are ignored).

$$V_{SA} = \frac{1}{2} R_{VDE} I_{gnd} \qquad \textit{Equ. III-1}$$

III.1.2 Current Source Description

The internal activity of a circuit corresponds to charge/discharge cycles which can be modelled by one or more current sources. The most basic description is that of a pulse waveform. This modelling approach has been adopted by the ICEM standard. A time-dependent waveform is assigned to the current source for transient analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear and single-frequency FM. In the schematic editor, the pulse is described, as shown in Figure 3- 2. The pulse description restricts the *Ib* shape to a periodic pulse, which is triangular if the pulse width parameter is set to zero.

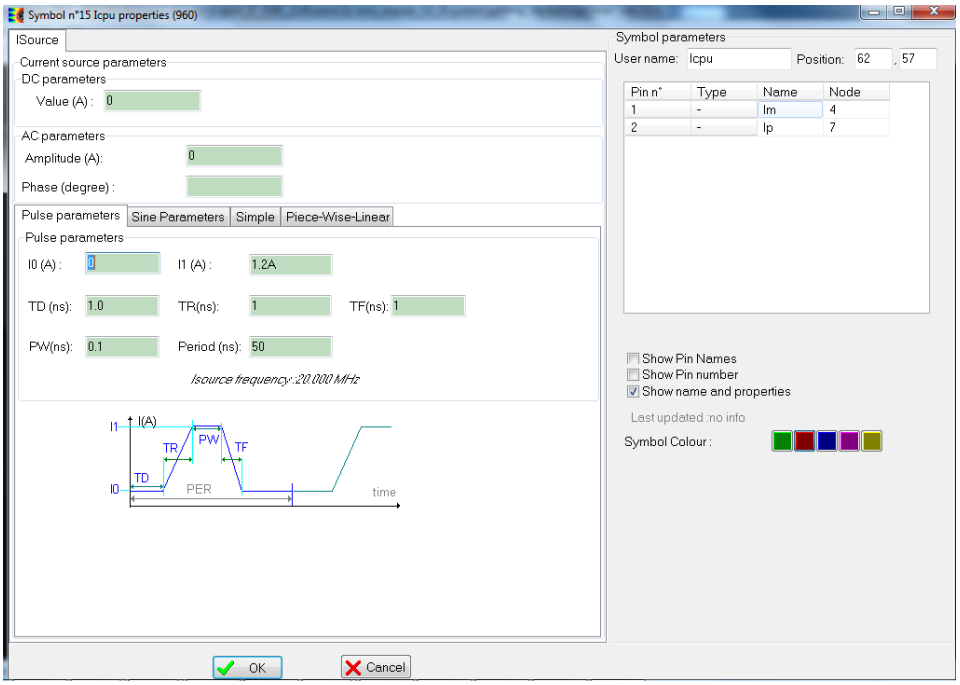


Figure 3- 2: Current Pulse parameters in the schematic editor (mpc_vde.sch)

```
PULSE(I0 I1 TD TR TF PW PER)
Example: IIcpu 5 7 PULSE(0 1.2A 1.0n 1n 1n 0.5n 50n)
```

Parameter	Description	Unit

I1	pulsed value	Amps
TD	rise time	TSTEP seconds
TF	fall time	TSTEP seconds
PW	pulse width	TSTOP seconds
PER	period	TSTOP seconds

Table 3- 2: Current source description under SPICE

III.1.3 Power supply Description

The power supply is modelled by a constant voltage source. In **Erreur ! Source du renvoi introuvable.**, the constant voltage source has a DC value of 3.0 V.

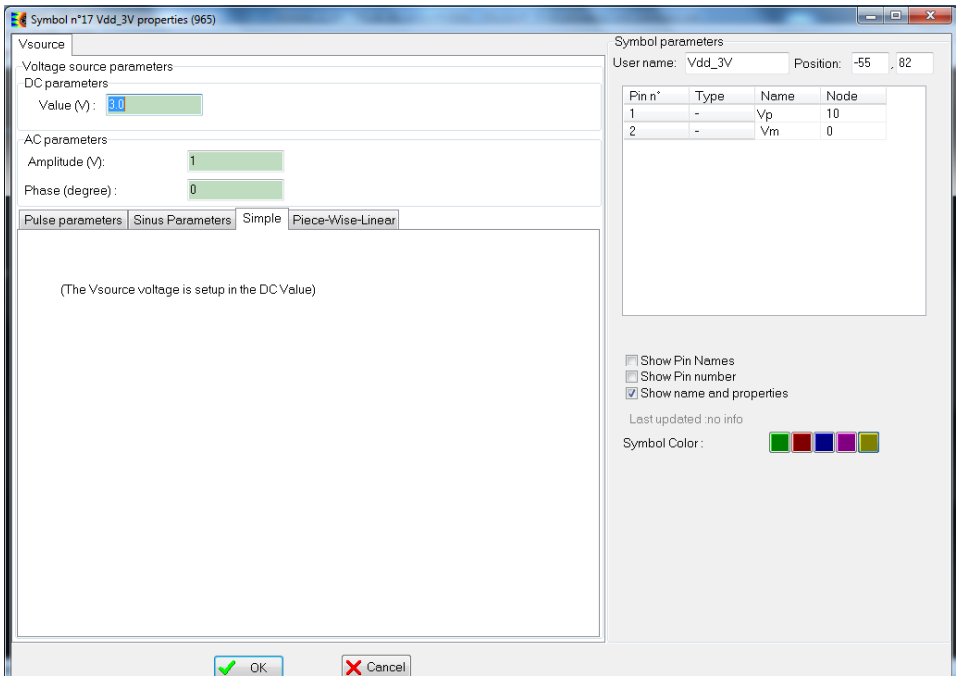


Figure 3- 3: Constant voltage source (examples\emission\mpc\mpc_vde.sch)

III.1.4 Analysis Description

In the editing window, a command line is added to set up the desired analysis. The line must start by '.TRAN' for a transient analysis. In Figure 3- 4, the time-domain analysis is set to 1000 ns, with a simulation step of 0.1 ns.

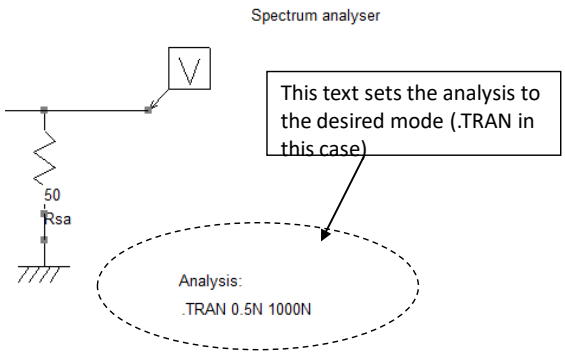


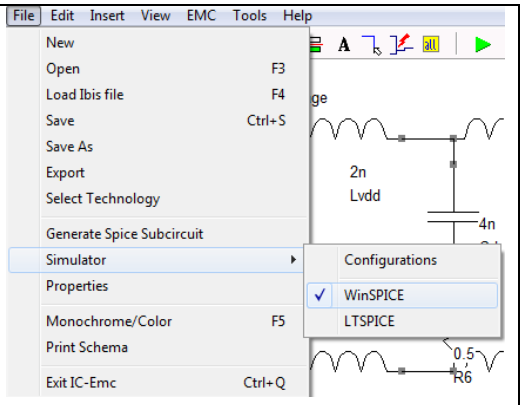
Figure 3- 4: Defining the SPICE simulation parameters

Two methods are used to insert an analysis line on the schematic:

- click on button **A** or in the "Edit > Text" menu, directly type the SPICE analysis command
- in the Insert menu, click on “Insert analysis line”. An interface dedicated to the configuration of the SPICE simulation is opened and the analysis line is automatically inserted on the schematic with the correct syntax.

III.1.5 Create the SPICE file

IC-EMC can build netlist files .cir compatible either with WinSPICE, Ngspice or LTSPICE. The selection of the simulator is made in the menu "File > Simulator". The simulator is launched either manually by the user or automatically after the generation of the netlist, depending on the selected options in the menu "File > Simulator > Configurations". In this example, we select WinSPICE as simulator. It will be launched manually: in the menu "File > Simulator > Configurations", select the option "Launch simulator manually".



Use command *File → Generate Spice file* or select <Ctrl>+<G> or click on the button in the command bar. The following screen appears (Figure 3- 5). This creates a file called “mpc_vde.cir”, which contains the circuit’s netlist description. This is the input file for the WinSPICE simulator.

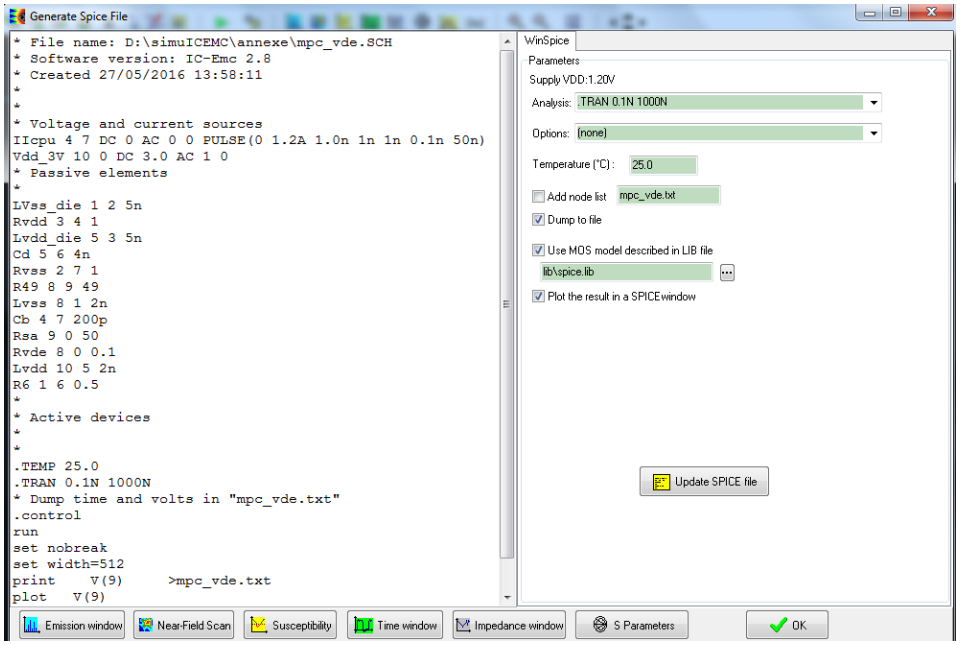


Figure 3- 5: The SPICE file generated from the schematic diagram (examples\emission\mpc\mpc_vde.sch)

III.1.6 Run SPICE Simulation

As explained in III.1.5, we select WinSPICE as SPICE simulator. We also choose to launch the simulator manually. Start the WinSpice program and click on "File > Open" (Figure 3- 6).

Select the desired .CIR file, i.e. the file generated by IC-EMC during the previous step (examples\emission\mpc\mpc_vde.cir). The simulation is performed in the time domain, and the following screen appears. The .TRAN analysis simulates the first 1000 ns of the transient evolution of the signal. The result is stored in a file called “mpc_vde.txt”. By default, the plot of the transient simulation appears in a new window shown in Figure 3- 6.

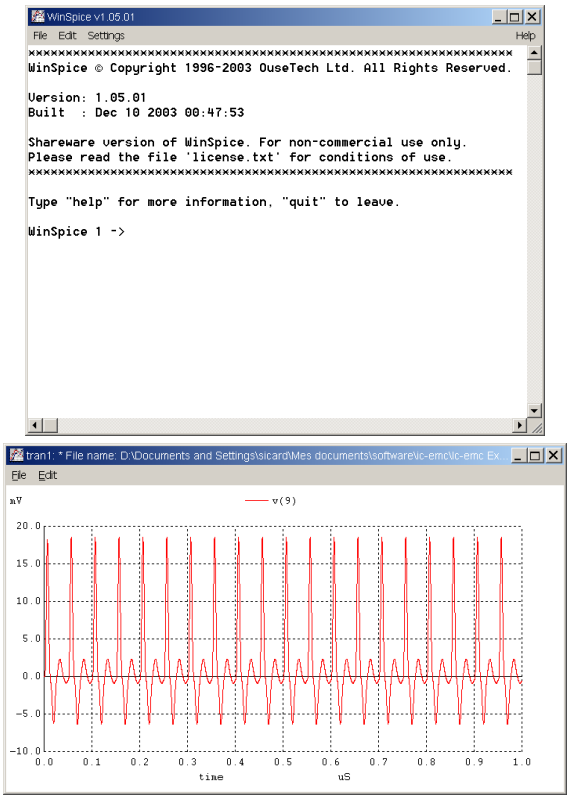


Figure 3- 6: The initial WinSPICE screen (top) and transient simulation performed by WinSPICE (bottom)

III.1.7 Plot the transient waveform

The transient waveform of the voltage across the 0.1 Ω resistor can be plotted in IC-EMC by clicking in the menu "EMC > Voltage vs. time" or on the button  in the command bar, as shown in Figure 3- 7. The list of signals saved by the simulator is given in the list Signals in the menu "Simulation Data" in the right part of the window. The signal name is "V(9)", where V indicates that we monitor a voltage, "9" is the number of the monitored node in the schematic.

Remark: click on the menu "View > View electrical net" or on the button  to display all the nodes directly on the schematic.

Right-clicking on the graph returns the (time ; voltage) coordinate of the clicking position. Moreover, if you move the cursor while you're right-clicking, when the right-click is released, the X-Y shift between the initial and stop positions is shown. Amplitude and period of signals may be evaluated with this method. More details about this window will be presented in III.6.

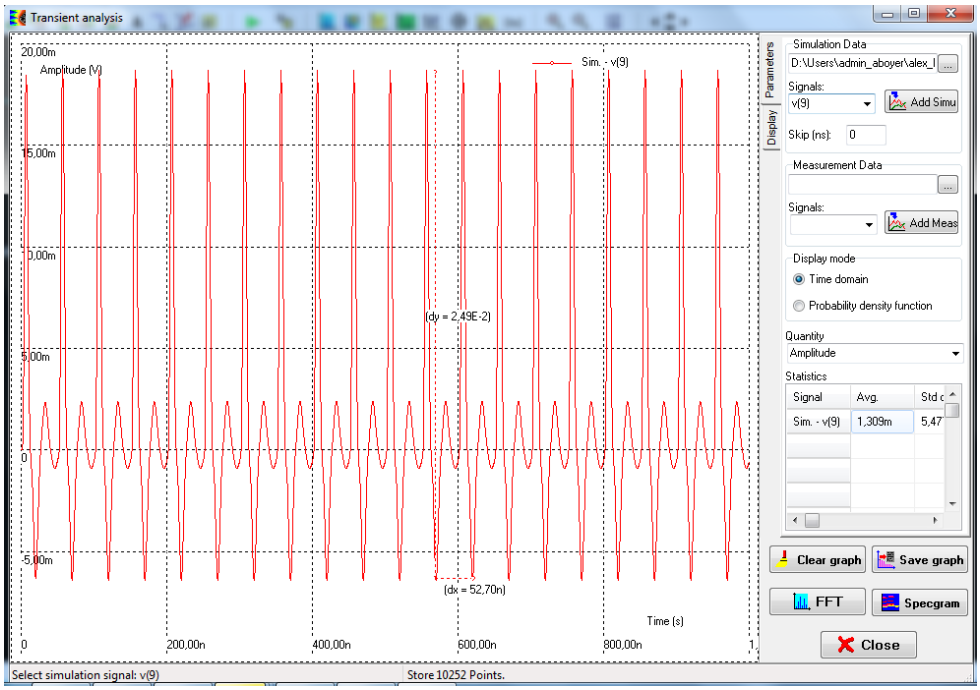


Figure 3- 7: Transient profile of the voltage induced across the 0.1 Ω resistor (examples\emission\mpc\mpc_vde.sch)

III.1.8 Emission simulation

The voltage waveform computed by the analogue simulator is translated into the frequency domain according to two methods:

- FFT mode: by default with a Fast Fourier Transform (FFT)
- EMI receiver mode: the effect of the intermediate frequency (IF) filter of an EMI receiver followed by a peak detector is simulated. The parameters of this mode should be set carefully because the computation time may be long.

The X-axis should cover the 1-5000 MHz range in a linear or logarithmic scale. The energy along the Y-axis is in dBµV or V (dBµA and A if results expressed in current are imported). In the command bar, click on button 'Emission vs. Frequency'  , or click "EMC > Emission vs. Frequency". A specific screen opens with Log/Log units configured to display voltage or current vs. frequency, as shown in Figure 3- 8. The main commands of this window are dispatched in several tabs:

- Input data: import of simulation (.txt from WinSPICE and Ngspice, and .raw from LTSPICE) and measurement result files (measured spectrum .tab and measured transient waveform .tran), save FFT of simulated or measured results.
- FFT Parameters: selection of the FFT mode or EMI receiver mode, selection of the FFT and EMI receiver parameters for simulation and measurement results.
- Display: set the axis configuration (limits, lin/log mode), visibility of curves on the graph, change color of displayed curves, plot envelop of spectrum,
- Simu Data and Meas Data: list of simulation and measurement results.
- Envelop & Limits: set parameters for the extraction of envelop of simulated or envelop spectrum, add a standard EMC limit.

By default, if the schematic is opened and if the SPICE simulation runs correctly, the FFT mode is selected. A FFT is performed and the simulation results are directly plotted when the window opens. If the result is not displayed, click the [...] button in “Simulation input data” part in the tab "Input data". Then select the file “mpc_vde.txt”. It is possible to remove the initial period of the simulated waveform, from 0 to the value in the field "Skip (ns)". If the simulation results are correctly imported, Figure 3- 8 presents the obtained results.

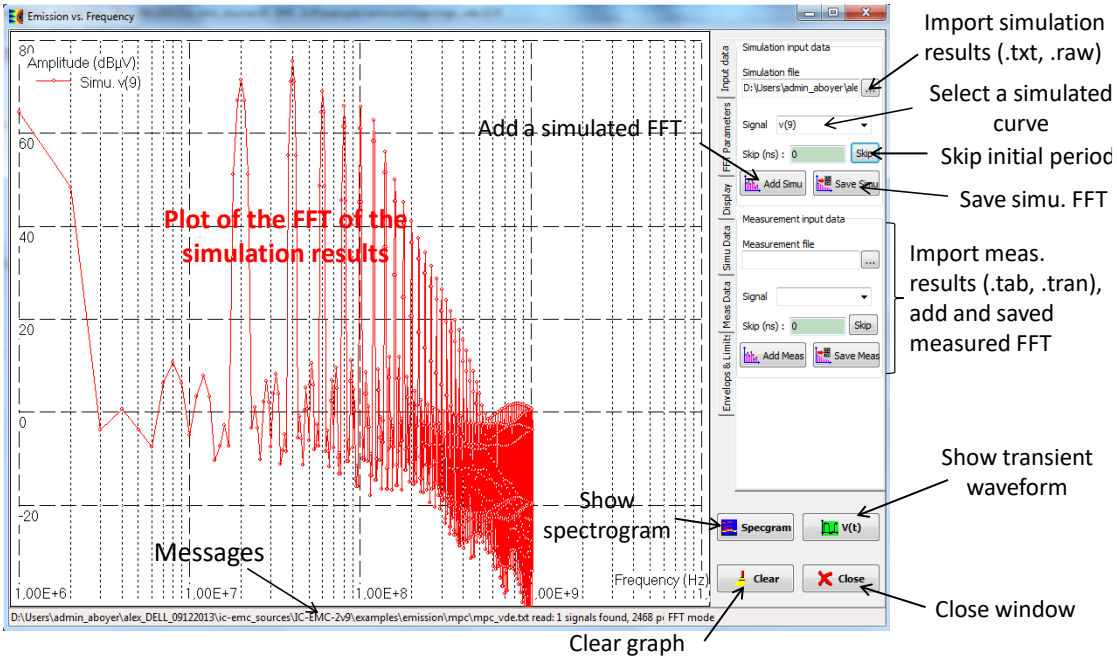
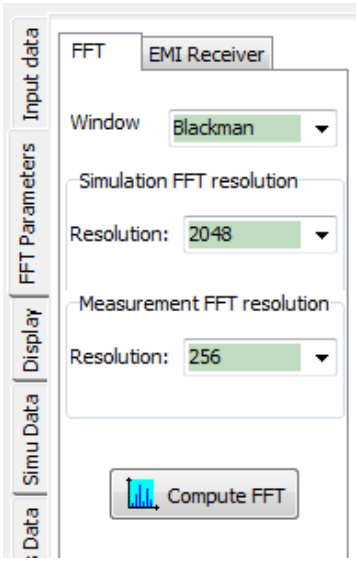


Figure 3- 8: Simulation of the microcontroller’s conducted emission (examples\emission\mpc\mpc_vde.sch)

The number of points N for the FFT (the FFT resolution) is a power of two and is adapted to fit the information included in the simulation and ensure the best resolution. Two FFT parameters can be adapted:

- the number of points or resolution of the FFT (maximum 262144)
- the windowing type: rectangular, Hamming and Blackman(Blackman by default)



The FFT resolution can be adjusted for the simulation and measurement results independently. The FFT resolution for the measurement results is visible only if a transient measurement results in .tran format has been imported. The number of points which form a displayed FFT result is equal to N/2. The frequency resolution Δf is given by equation I-2 and the maximum frequency F_{max} by equation I-3.

$$\Delta f = \frac{1}{T_{\max}} = \frac{1}{NT_e} \qquad \textit{Equ. III-2}$$

$$F_{\max} = \frac{1}{2T_e} \qquad \textit{Equ. III-3}$$

where T_e is the sampling period of the transient signal, T_{max} the duration of the transient signal.

III.1.9 Comparison with Measurements

In the "Input data" tab, click the [...] button in “Measurement input data” and select the file " examples\emission\mpc\mpc_vde.tab”. Then click on the button "Add meas." to display the measured spectrum. Figure 3- 9 shows the comparison between measurements and simulations.

The measurement curve is actually the envelop of the measured spectrum. The simulation fits the measured data up to 260 MHz except at 120 MHz, where the simulation is 10 dB above the measurement. Despite the discrepancy around this frequency, an acceptable correlation is obtained with a very simple model. Correlation with measurements may be improved, especially at high frequencies, by modifying the current profile, the IC internal power supply network and board models.

The axis settings and the curve properties can be modified by changing the options available on tab Display.

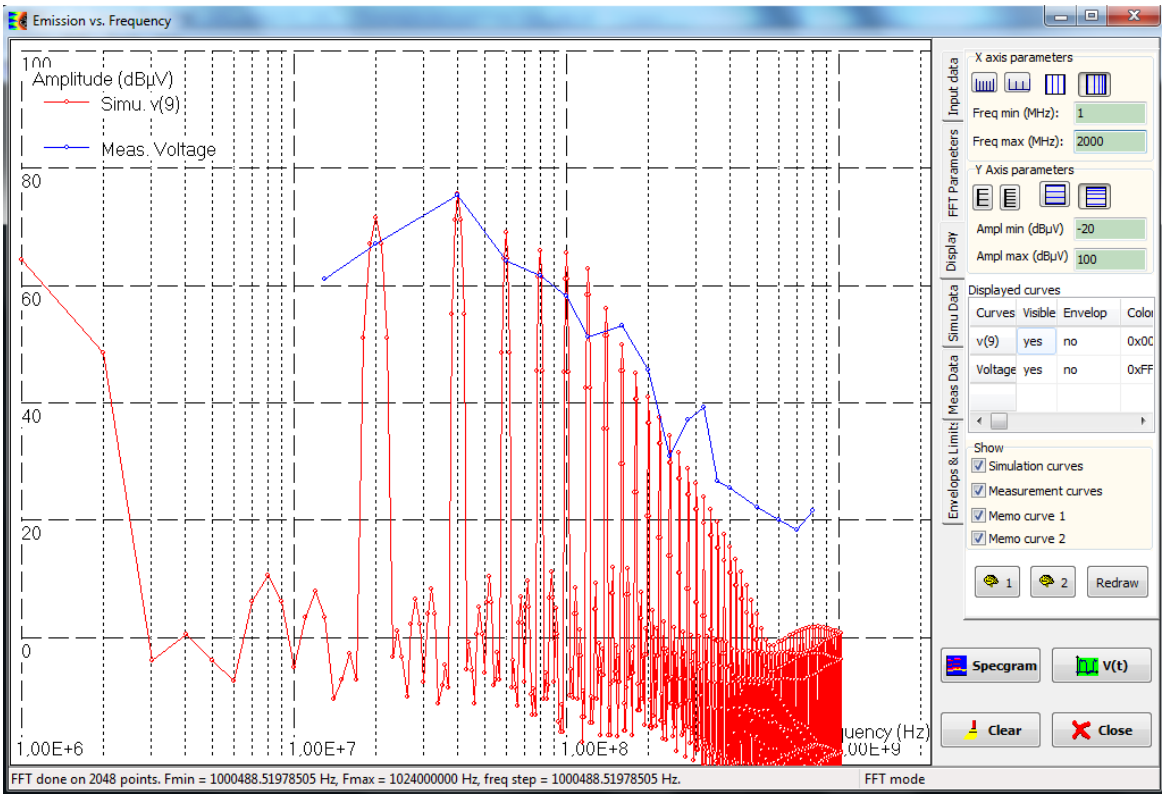


Figure 3- 9: Comparison between measured and conducted emission for a microcontroller (mpc_vde.sch, mpe_vde.tab)

III.2 Impedance analysis of the power supply network of a circuit mounted in a 64 BGA package

This example presents the flow to simulate the impedance profile in frequency domain of the passive decoupling network (PDN) of a small 90 nm circuit mounted in a 64 ball grid array (BGA) package. The PDN is a macroscopic block defined by ICEM standard [ICEM] to describe the passive network which exists between several IC accesses, e.g the power supply network of a circuit. The accuracy of the PDN model is fundamental for emission and susceptibility predictions as it influences directly the noise propagation within the circuit. PDN modeling can be done either from Z parameter or S parameter representation.

In IC-EMC, impedance analysis is intended for rapid simulation of the impedance Z(f) for single port devices. For multiport analysis or conversion to S parameter, it is advised to perform S parameter simulation, which is described in part III.3.

III.2.1 Load the example

Load the file called "examples/impedance/FFIO90/ FFIO_90nm_Z_VDDE.sch". The electrical schematic is shown in Figure 3- 10. The schematic models the PDN of a small test chip fabricated in CMOS 90 nm containing several I/O structures [Boy08].

The circuit is mounted in a 64-pin BGA package, as described in Figure 3- 11.

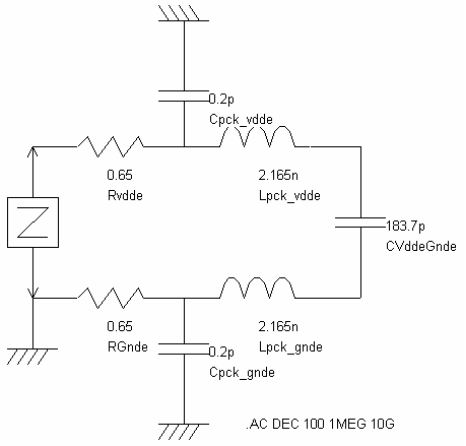


Figure 3- 10: PDN model of a test chip fabricated in CMOS 90 nm containing I/O structures (examples/impedance/FFIO90/ FFIO_90nm_Z_VDDE.sch)

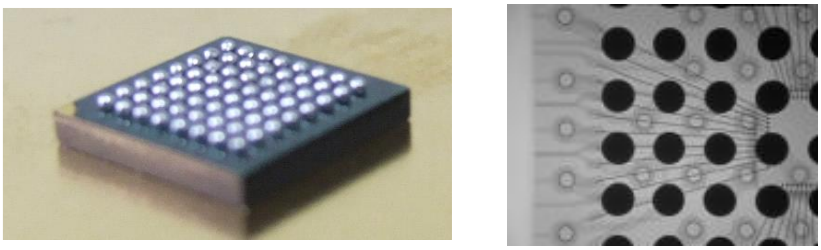


Figure 3- 11: 64-pin LBGA package [Boy08]

Measurements have been performed using a Vector Network Analyzer (VNA) directly on the package balls with a coplanar probe placed between adjacent power pins VDDE and GNDE. The model has been extracted from the S parameter measurements. The PDN model includes two parts:

- the die contribution, i.e. interconnections and on-chip decoupling capacitances
- the package contribution, i.e inductive effects of balls, vias and bonding wires constituting the BGA package

Table 3- 3 gives details of the elements of the model.

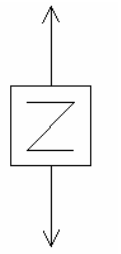
Parameters	Description	Remarks
CVddeGnde	Equivalent on-chip capacitance Unit: Farad Description: discrete capacitance	This element models all parasitic and intentional on-chip capacitances between power supply VDDE and ground GNDE access.
Lpck_vdde, Lpck_gnde	Package parasitic inductance Unit: Henry Description: discrete inductance	These 2 inductances model the contribution of all elements of VDDE and GNDE pins. With on-chip capacitance, they are responsible of the first resonance.
Cpck_vdde, Cpck_gnde	Package parasitic capacitance Unit: Farad Description: discrete capacitance	These 2 capacitances model the contribution of all elements of VDDE and GNDE pins. They are added to model the package self resonance which appears above several GHz.
RVdde, RGnde	Total power supply and ground resistance Unit: Ohm Description: discrete resistance	These resistors represent the resistive contribution of package and on-chip interconnections. Their effect is negligible except at resonance frequency.

Table 3- 3: Details of basic elements of FFIO_90nm_Z_VDDE.sch

III.2.2 Impedance probe description

The impedance analysis corresponds to a simulation of the input impedance (also written Zin or Z11) seen from one circuit access relatively to a reference. In this example, the access is the power supply pin VDDE. The measurement is referenced to the ground pin GNDE.

Impedance simulation is allowed only if an impedance probe or Z probe is placed in the schematic diagram. The Z probe (Figure 3- 12) is accessible from the palette. If you double click on the Z probe, the property screen is displayed, but without any specific property. However, the Z probe is not a transparent symbol. When placed on the schematic, it creates a voltage source with the description below:



```
VZ 1 2 DC 0 AC 1 0
…..
plot (V(1)-V(2))/I(VZ)
```

Figure 3- 12: Impedance probe and associated SPICE description

The voltage source associated to the Z probe is an AC source with an amplitude of 1 V. As may be found at the end of the SPICE netlist, a “plot” control is associated with an equation which computes the impedance by dividing the voltage amplitude across the probe by the current provided by the impedance probe.

Remark: use only one impedance probe per schematic diagram. The input impedance is linked to the current that a perfect voltage source delivers to a circuit. If a second AC voltage source is present, it will modify the current which flows along the branch of the first Z probe and hence the computed impedance.

III.2.3 Analysis description

Impedance simulation is a small signal frequency analysis, so that it requires an AC simulation. The command line: " .AC DEC 100 1MEG 10G" is added to set up the desired analysis. The text must start by '.AC' followed by the AC simulation parameters. The frequency sampling is logarithmic (option DEC) with 100 points per decade between 1 MHz and 10 GHz. Two methods are used to insert an analysis line on the schematic:

- click on button A or in the "Edit > Text" menu, directly type the SPICE analysis command
- Click on "Insert > Insert analysis line". An interface dedicated to the configuration of the SPICE simulation is opened (Figure 3- 13) and the analysis line is automatically inserted on the schematic with the correct syntax.

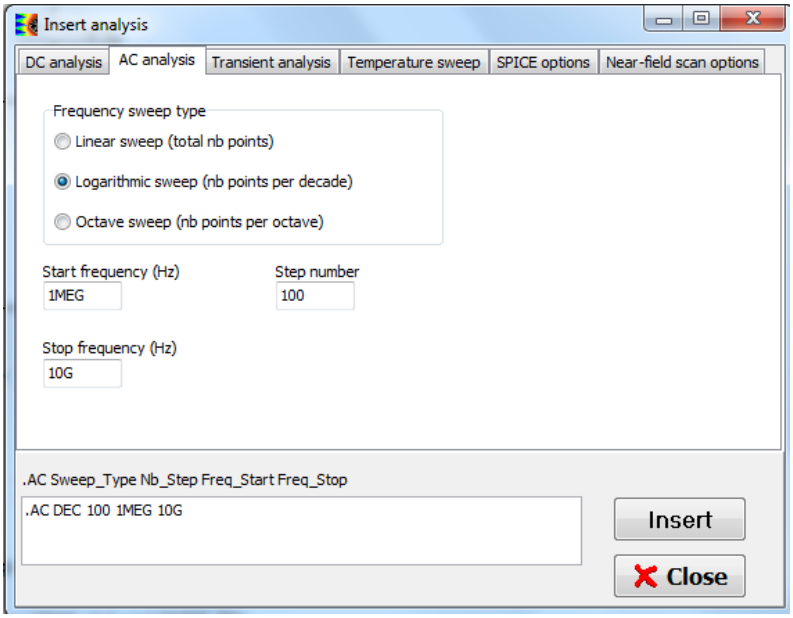


Figure 3- 13: Insert AC simulation command line on the schematic ("Insert > Insert analysis line")

III.2.4 Run SPICE simulation

In this example, WinSPICE is used as simulator. In the menu "File > Simulator", select "WinSPICE". Then, click on "File > Simulator > Configurations" to set the options of the simulators. The right window of Figure 3- 14 opens. The upper part gives the access path of the simulator. They have to be set up correctly before any simulation. In the lower part, three simulator launching options are proposed:

- Launch simulator manually: when the user generates SPICE netlist , he has to launch the simulator, opens the circuit netlist (.cir file) and launch the simulation
- Interactive mode: when the user generates SPICE netlist , the simulator is automatically launched and remains opened at the end of the simulation to analyze the result
- Batch mode: when the user generates SPICE netlist , the simulator is automatically launched but is closed directly at the end of the simulation

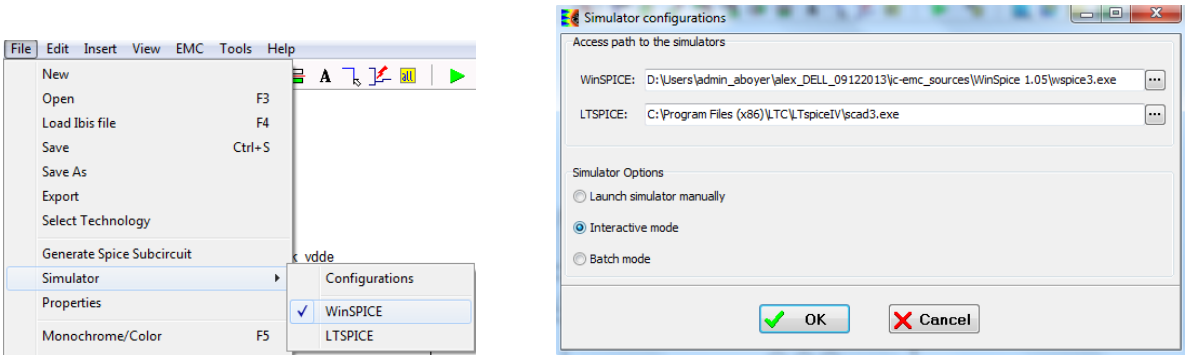


Figure 3- 14: Select simulator and configure the simulator options

In this example, select "Interactive mode" and click on the button OK. The simulator options are kept for the next simulations, until you change them.

Use command *File → Generate Spice file* or click on the button in the command bar. The SPICE netlist FFIO_90nm_Z_VDDE.cir is generated. WinSPICE is automatically launched and the impedance simulation is done. The following screen appears. WinSPICE can be closed at the end of the simulation.

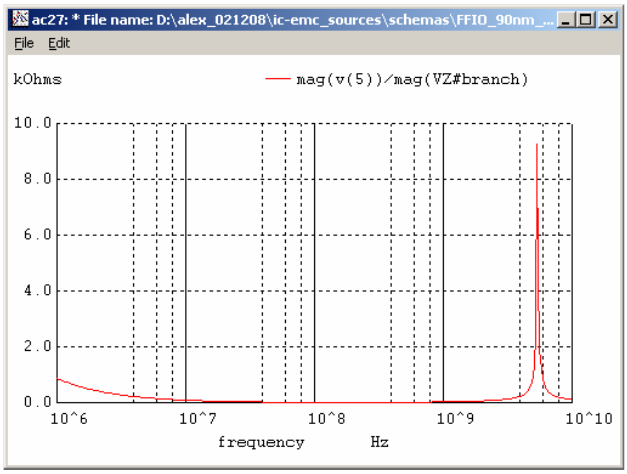


Figure 3- 15: AC simulation performed by WinSPICE (FFIO_90nm_Z_VDDE.txt)

III.2.5 Impedance analysis

The impedance profile vs. frequency computed by WinSPICE can be displayed in a specific screen dedicated to impedance analysis. In the SPICE generator menu, click "Impedance Window", or click "EMC" → "Impedance vs. Frequency". Alternatively, you may click the icon . A specific screen with Log/Log units configured to display impedance vs. frequency is proposed, as shown in Figure 3- 16.

The main commands of this window are dispatched in several tabs:

- Parameters: X-Y axis configuration (lin/log display mode), add basic R, L, C impedance profile
- Display: display simulation, measurement, recorded results
- Freq: list of simulation and measurement results

By default, if the schematic is opened and if the SPICE simulation runs correctly, the Z(f) profile is plotted. If the result is not displayed, click the [...] button on the right of “SPICE simu” and select file “FFIO_90nm_Z_VDDE..txt”.

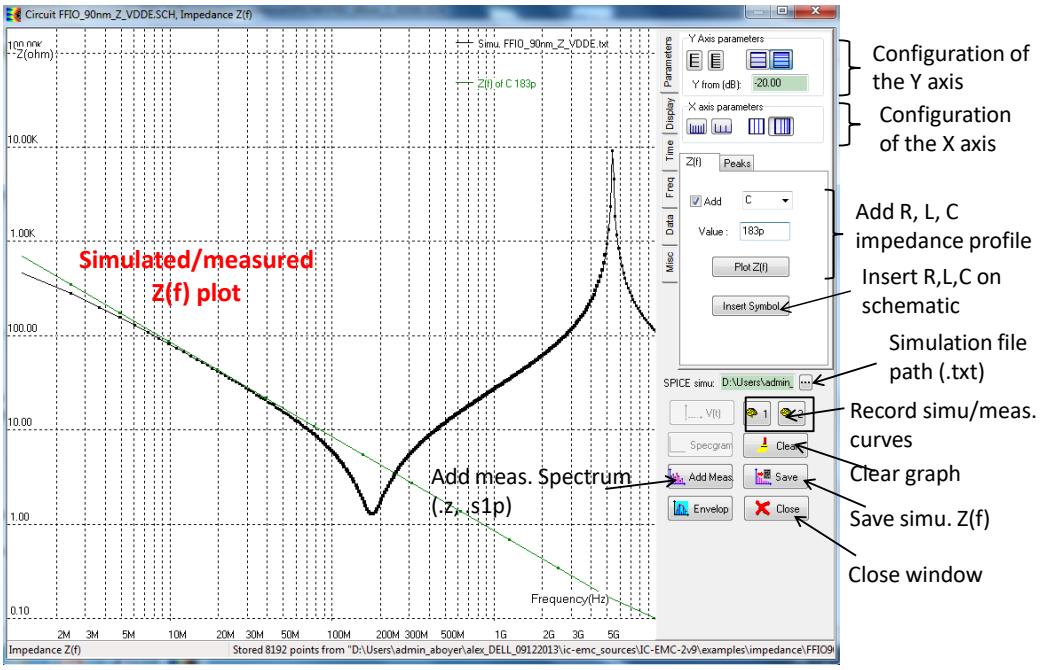


Figure 3- 16: Input impedance simulation performed by WinSPICE (examples/impedance/FFIO90/ FFIO_90nm_Z_VDDE.sch)

At low frequency, impedance tends to decrease due to the on-chip capacitance effect. At 180 MHz, the first resonance linked to the on-chip capacitance and the package inductances appears. A second resonance due to package inductance and capacitance appears at 5.4 GHz.

To verify the on-chip capacitance of the circuit from the Z(f) profile, click on the box "Add" in the tab Z(f) and select C. Type 183 pF in the field "Value" and click on the button "Plot Z(f)". The Z(f) profile of a 183 pF is displayed and is tangent to the Z(f) profile of the circuit PDN in low frequency. It confirms that the total on-chip capacitance is about 183 pF. This basic tool can also be used with Z(f) measurement to extract equivalent resistance, capacitance or inductance.

III.2.6 Comparison with measurement

In the impedance window, click on the button “Add Meas” to display the impedance measurement of the PDN of the circuit. The measurement data are available in the file called “examples/impedance/FFIO90/Z11_FFIO_VDDE_A4B5.z”. The comparison between measurement and simulation is presented in Figure 3- 17 and proves the validity of the model up to 3 GHz.

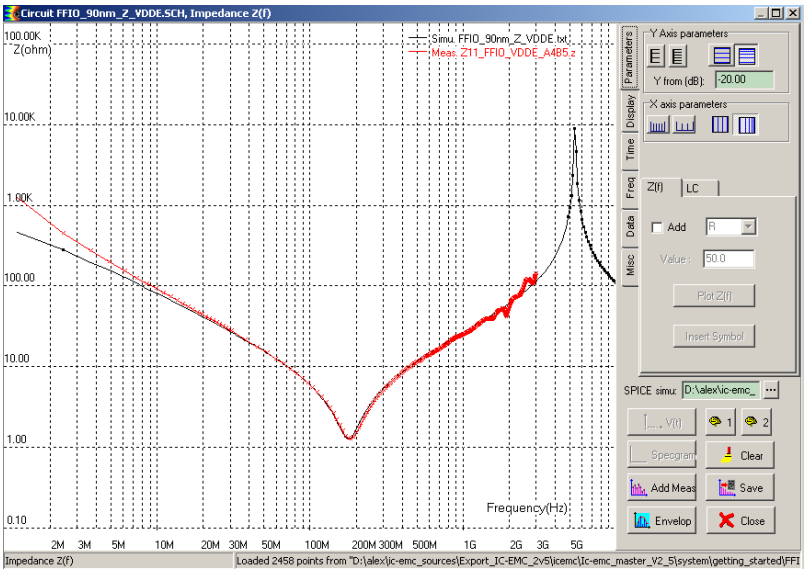


Figure 3- 17: Comparison between measured and simulated input impedance of the PDN of the 90 nm circuit (examples/impedance/FFIO90/ Z11_FFIO_VDDE_A4B5.z)

III.3 S parameter analysis for model construction of a bias tee

A typical method to construct electrical models of components is based on equivalent R, L,C networks extracted from S parameter measurements. Here, we present an example of comparison between measurements and simulations of two-port S parameter done on a home-made bias tee. A bias tee is a three-port decoupling network used to superimpose a low frequency signal and a high frequency signals. The bias tee ensures the isolation between the low frequency and the high frequency signal sources. A bias tee is required in IEC62132-4 Direct Power Injection (DPI) test in order to superimpose a conducted aggression on a low frequency signal (input signal or power supply). The name given to the three ports of the bias tee are:

- a low frequency (LF) input
- a radiofrequency (RF) input, connected to the RF disturbance source
- the output with the signal resulting of the superposition of both inputs

The LF input is isolated from RF signal by a resistor, inductor or ferrite which filter high frequency signal. Resistors should be avoided if DPI is conducted on a power supply because of the power dissipation. The RF input is isolated from low frequency signal by a series capacitor. Figure 3- 18 presents a bias tee dedicated to DPI test on the frequency range 10 MHz – 3 GHz. It is build with several passive devices mounted on a PTFE substrate board. Input and output SMA connectors are connected by 50 Ω microstrip line. A 1 nF capacitor and a 1 µH inductor isolate RF and LF input from each other.

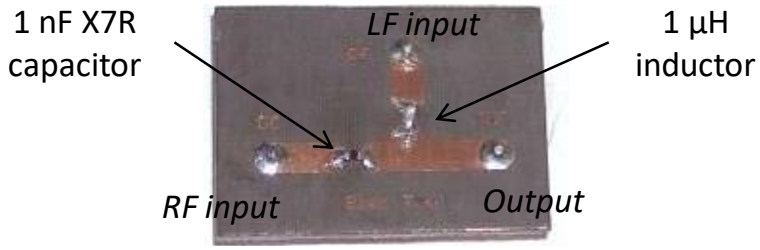


Figure 3- 18: Home-made bias tee for DPI tests

Values of inductors and capacitors are chosen in order to give the three following properties to the bias tee:

- A small reflection coefficient at RF input over all the targeted frequency range. It should be inferior to -10 dB to reduce input return loss.
- A high isolation or transmission coefficient from RF input and LF input over all the targeted frequency range. It should be less than -10 dB to prevent from RF leakage to LF source.
- A high transmission coefficient from RF input to output over all the targeted frequency range. It should be greater than -3 dB to enhance RF transmission to the output.

III.3.1 Load the example

Open the file "examples\emc_lib\3_port_bias_tee.sch". The schematic is shown in Figure 3-19. Models of microstrip line are lossless 50 Ω transmission line, their delay time have been computed from physical length and dielectric constant of the substrate. The capacitor and inductor models have been extracted previously. A parasitic serial inductor is added to the capacitor while a parallel capacitor is added to the inductor to induce self-resonance. Resistances are added to reduce their quality factors. Three S parameter probes are placed at each terminal of the model so that a full 3×3 scattering matrix can be simulated.

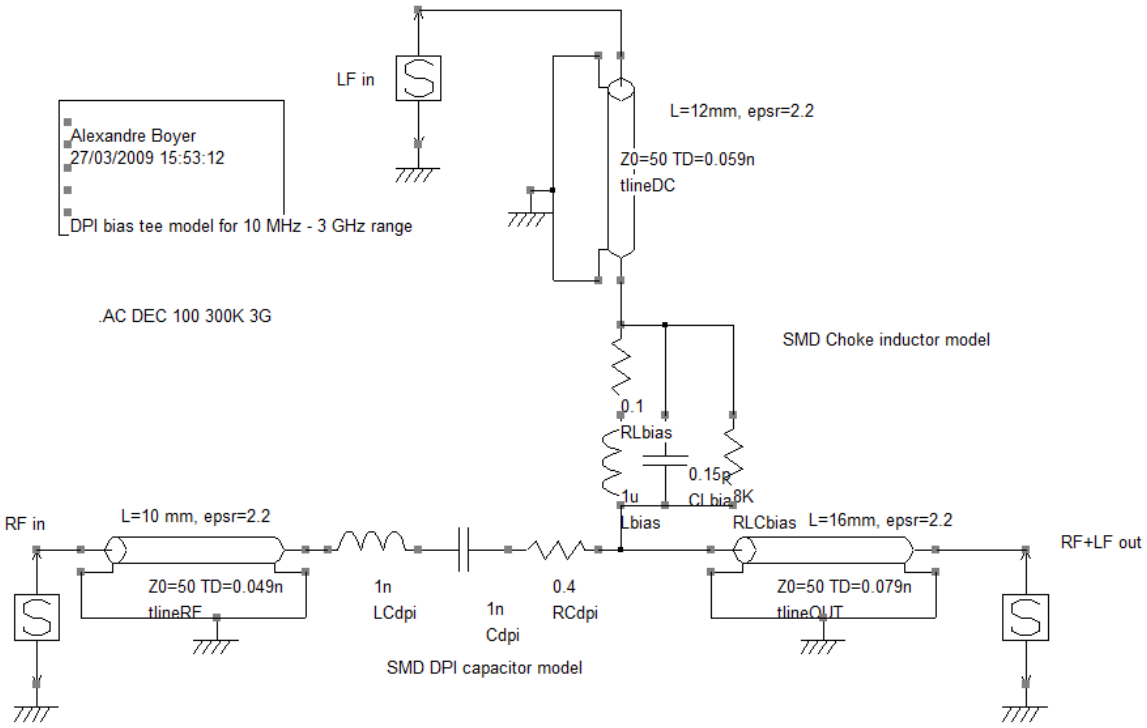


Figure 3- 19: Model of a bias tee optimized for the frequency range 10 MHz – 3 GHz (examples\EMC_lib\3_port_bias_tee.sch)

III.3.2 S parameter probe description

S parameter simulation is allowed only if at least one S parameter port probe is placed within the schematic. The S parameter probe is accessible from the palette with the symbol  . Double clicking on the probe opens their property screen (Figure 3- 20). A S parameter probe is characterized by a user name, a unique number, a characteristic impedance *Z0* (which must be common to every port) and a DC voltage. A port can be disabled so that it is replaced by a resistance with a value of *Z0*.

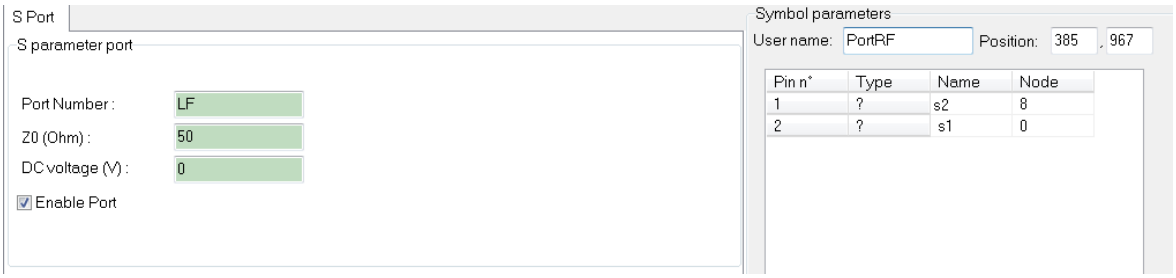


Figure 3- 20: S parameter port probe properties

A S parameter probe is formed by a sine waveform voltage source with a series resistance Z0. The amplitude of the voltage source is equal to 0 or 1 V depending if the probe is activated or not. Figure 3- 21 presents a representation of a 2-port device characterized by S parameters. S parameter probes are composed of small signal sinusoidal source and reference impedance Z_0 connected to device terminals.

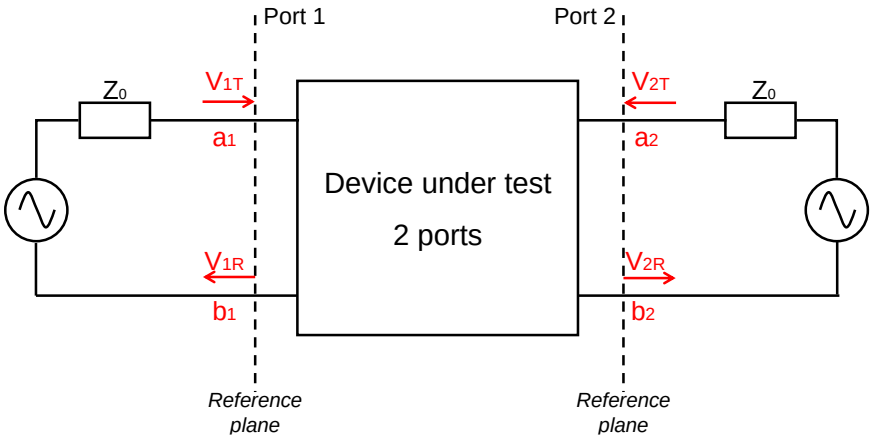


Figure 3- 21 : S parameter characterization of a 2 port device

The four parameters, listed below, allow a complete characterization of power exchanges between the 2 ports. They form the S parameter matrix. This principle can be extended to device with any port number.

Input reflection coefficient $S_{11} = \frac{b_1}{a_1}\Big\|_{a_2=0}$ No power fed from port 2. Port 2 terminated by Z0 to prevent from reflection at port 2.	**Output reflection coefficient** $S_{22} = \frac{b_2}{a_2}\Big\|_{a_1=0}$ No power fed from port 1. Port 1 terminated by Z0 to prevent from reflection at port 1.
Forward transmission coefficient $S_{21} = \frac{b_2}{a_1}\Big\|_{a_2=0}$ No power fed from port 2. Port 2 terminated by Z0 to prevent from reflection at port 2.	**Forward transmission coefficient** $S_{12} = \frac{b_1}{a_2}\Big\|_{a_1=0}$ No power fed from port 1. Port 1 terminated by Z0 to prevent from reflection at port 1.

Table 3- 4 : Definition of the S parameters for a 2 port device

S parameter matrix can be converted into other forms (impedance, admittance, ABCD …). For electrical modeling purpose, impedance is a convenient representation. The conversion between [S] to [Z] parameter matrices is given by the following equation, where [I] is the identity matrix.

$$[Z] = Z_0 \frac{[I]+[S]}{[I]-[S]} \qquad \textit{Equ. III-4}$$

Remarks: if other probes (e.g. voltage, current or impedance probes) are present on the schematic, S parameter analysis is cancelled. Internal voltage source amplitude is set to 0 V, so each port is loaded by 50 ohms. The number of ports is limited to four. If more ports are added, they will be ignored and will be replaced by 50 Ω resistances.

III.3.3 Analysis description

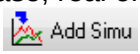
S parameter simulation requires a small signal or AC simulation. A text line is added on the schematic which sets up the desired analysis. The text must start by '.AC' followed by the AC simulation parameters. In Figure 3- 19, the frequency sampling is logarithmic, with 100 points per decade between 300 KHz and 3 GHz. The analysis line can also be inserted with the command 'Insert' → 'Insert analysis line'. Two methods are used to insert an analysis line on the schematic:

- click on button  or in the "Edit > Text" menu, directly type the SPICE analysis command
- Click on "Insert > Insert analysis line". An interface dedicated to the configuration of the SPICE simulation is opened and the analysis line is automatically inserted on the schematic with the correct syntax.

III.3.4 Run SPICE simulation

Select WinSPICE as simulator in "File > Simulator". In the menu "File > Simulator > Configurations", select "Interactive mode" to launch SPICE simulation automatically after the SPICE netlist generation  .

III.3.5 S parameter analysis

Click "EMC > S parameters" to open the [s] parameter display screen. Alternatively, you may click the icon  . A specific screen with a blank screen and a menu on the right appears. Simulation results can be plotted by selecting the quantity to plot (S11, S12, …) and its format (magnitude, phase, real or imaginary part) in the "Simulation data" part and clicking on the button "Add Simu" 

. The graph can be plotted either in cartesian or Smith chart mode ("Display mode"). The result can be converted either in S or Z parameters, or mixed-mode parameters when 2 or 4 ports are placed on the schematic ("Conversion") (an example with mixed-mode S parameters is given in III.9.2). The X and Y axes boundaries and lin/log format can be set in "X axis" and "Y axis" parts.

In order to check the three properties of bias tee listed in III.3, set the format to "Mag (linear)", select successively the quantities "SRFRF", "SRFLF" and "SRFOUT" an click on "Add Simu" to plot the RF input reflection coefficient, the RF-LF isolation and the RF to OUT transmission respectively. In "Display mode", select "Cartesian", and choose "S" in "Conversion" to plot S parameters. In "X axis" and "Y axis" parts, check the box "Log" to plot the axes in logarithmic mode. Figure 3- 22 shows the result that you should obtain.

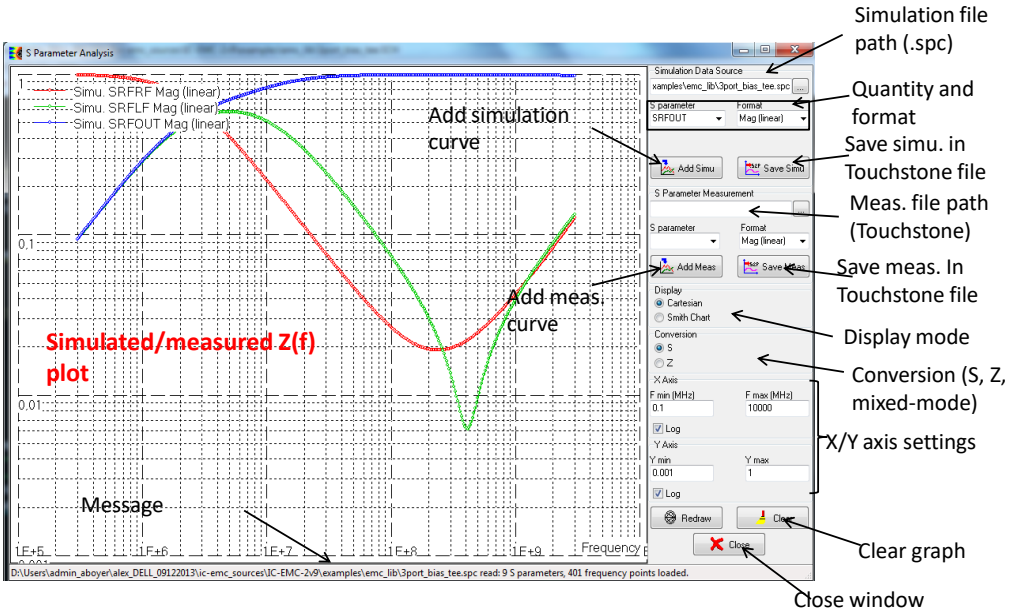


Figure 3- 22: S parameter simulation of a three port bias tee (examples\EMC_lib\3_port_bias_tee.sch)

The simulation shows that the RF input reflection coefficient (SRFRF parameter) is low between 10 MHz and 3 GHz while the transmission coefficient from RF to OUT terminals (SRFOUT parameter) is nearly equal to 1. The bias tee ensures an efficient transfer of the RF energy to a 50 Ω load connected to the output of the bias tee. The transmission coefficient between RF and LF terminals (SRFLF) is also small between 10 MHz and 3 GHz, proving the good isolation between the RF and LF sources.

The results can be plotted in Z parameter format if you select "Z" in "Conversion part". Click on the button "Redraw" to fit automatically the X and Y axes boundaries. The curves shows respectively the RF input impedance (ZRFRF parameter), the RF to LF and RF to OUT transfer impedances (ZRFLF and ZRFOUT parameters).

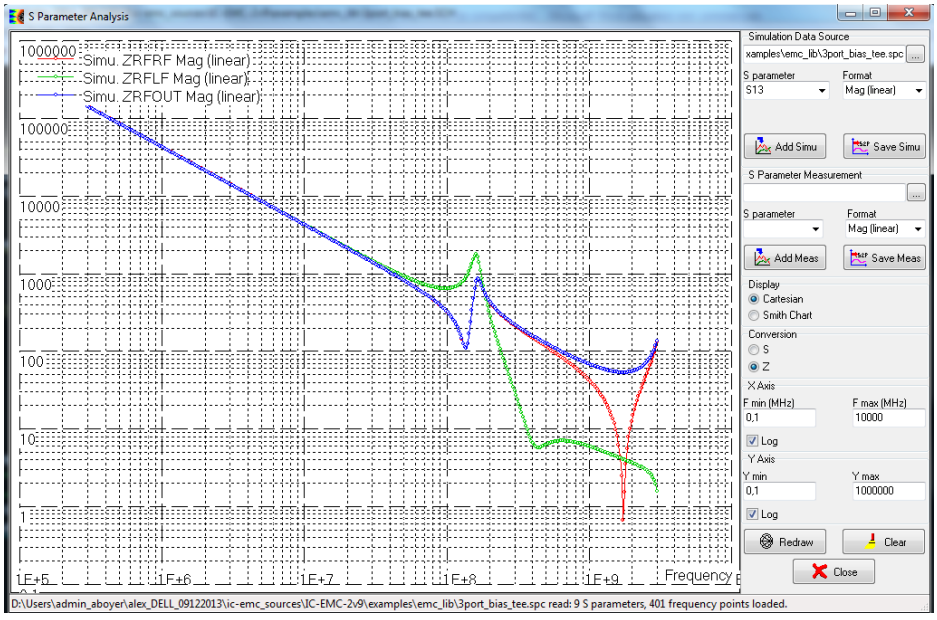


Figure 3- 23: Conversion from S to Z parameters (examples\EMC_lib\3_port_bias_tee.sch)

The simulation results can be exported in the common Touchstone format .snp, where n is the number of ports and is limited to 4 in IC-EMC. Click on the button "Save Simu." and type the name of the exported file. As there are three ports, the file is saved in a .s3p file.

III.3.6 Comparison with measurement

In the "S parameter measurement" part, click on the button  to import measurement files. They are in Touchstone format .s1p, .s2p, .s3p or .s4p. The tool can import measurements with up to four ports. Import the file xxx, select the quantity in "S parameter" list and the format in "Format" list. Finally, click on the button "Add meas." to plot the measurement results, as shown in the figure below.

III.4 Simulation of the conducted immunity on the power supply of a microcontroller

This example aims at presenting the flow to simulate the susceptibility of a circuit to radiofrequency interference (RFI). In this short case study, a sine wave disturbance is conducted on the power supply network of a digital circuit until the noise level measured on the pin of an output buffer exceeds a predefined noise margin. The circuit under test is a 16-bit microcontroller (HCS12X or S12X from Freescale Semiconductor). Conducted emission measurements are related to the standard IEC 62132-3 Direct Power Injection (DPI) method [IEC62-4]. The test covers the frequency range from 1 to 1000 MHz. The immunity model is based on an equivalent R,L,C circuit modeling the power distribution network (PDN) of the circuit, which was extracted from [s] parameter measurement.

III.4.1 Load the S parameter simulation model

Load the file called “examples\immunity\S12X_RFI\S12XPowerSupply_S11.sch”, as described in Figure 3- 24. The model has been extracted by a vector network analyzer measurement from 300 KHz up to 3 GHz, which has been performed through a SMA connector on the power supply plane. It provides a simplistic version of the equivalent electrical model of the PDN of the microcontroller between power supply VDDR and ground VSSR pins. A S parameter probe is placed between VDDR and VSSR pins in order to perform a simulation of the impedance connected between these pins. Information about the elements of the model is given in Table 3- 5. The measured S11 parameter used to extract this model is given in the file S12XPowerSupply_S11Meas.s1p. Refer to part III.3 to simulate the impedance of the microcontroller's PDN and compare it with measurements.

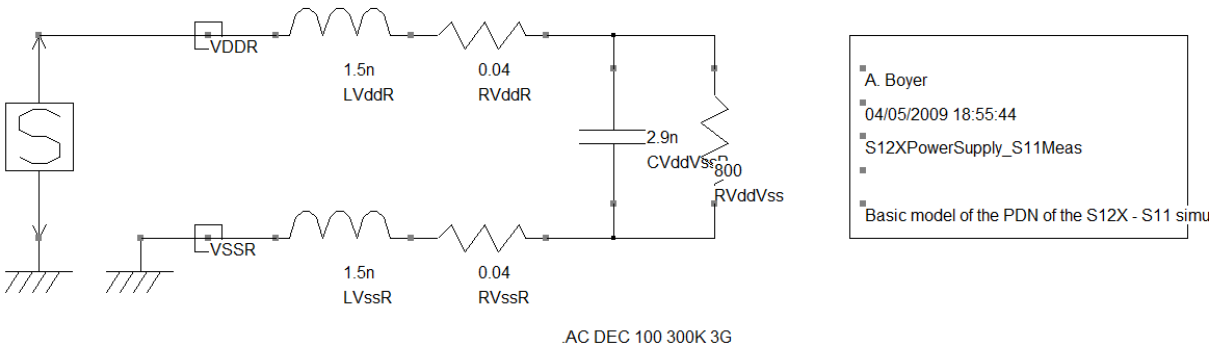


Figure 3- 24: Basic PDN model of the S12X microcontroller (examples\immunity\S12X_RFI\S12XPowerSupply_S11.sch)

Parameters	Description	Remarks
LVddR, LVssR	Package and board parasitic inductance Unit: Henry Description: discrete inductance	These 2 inductances model the contribution of all the Vdd and Vss pins of the S12X package and the parasitic inductance of power supply and ground planes of the board
RVddR, RVssR	Package and board parasitic resistance Unit: Ohm Description: discrete resistance	These resistors represent the resistive contribution of all the elements between Vdd and Vss (board, package, die).
CVddVssR	Circuit and board capacitance Unit: Farad Description: discrete capacitance	This capacitance models the total capacitance between Vdd and Vss. It is the sum of board interplane capacitance and all the on-chip capacitances between Vdd and Vss
RVddVssR	Loss resistance Unit: Ohm Description: discrete resistance	This resistance is added between Vdd and Vss and models all the dielectric losses between power and ground plane and on-chip leakage between Vdd and Vss

Table 3- 5: Details of basic elements of S12XPowerSupply_S11.sch

III.4.2 Load the susceptibility simulation model

A basic susceptibility to RFI model is built from the extracted PDN. Load the file “examples\immunity\S12X_RFI\RFI_S12XPowerSupply.sch” described in Figure 3- 25. This schematic models the conducted injection of RFI in the power plane of the S12X board according to the IEC 62132-3 DPI standard. The susceptibility of the circuit is evaluated according to the RF noise coupled on the pin of an output buffer of the microcontroller and measured with an oscilloscope. The output buffer is tight to a 5 V voltage. The circuit is considered failed when the amplitude of noise measured with the oscilloscope exceeds 1 V (20 % of the supply voltage).

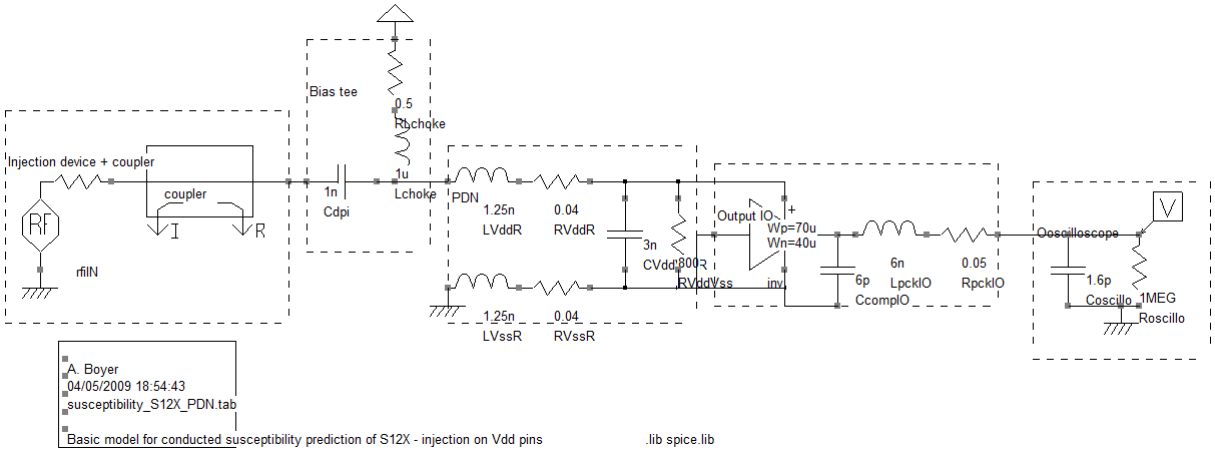


Figure 3- 25: Basic model for conducted susceptibility prediction of the S12X microcontroller (examples\immunity\S12X_RFI\RFI_S12XPowerSupply.sch)

Several new elements have been added in the schematic, which are detailed in Table 3- 6.

Elements	Description
Injection device and coupler	The injection device is used to produce the RF disturbance and consists in a sinusoidal source with a 50 ohms output resistor. Frequency and amplitude of the RF disturbance varies during simulation and are controlled by user defined parameters. A coupler is added in the model to measure the forward power required to induce a failure. See chapter 7 for more information about susceptibility simulation.
Bias tee	This element composed of an injection capacitor and a choke inductance is required to superimpose a RF disturbance to a low frequency signal (e.g. the power supply voltage).
Power decoupling network (PDN)	A simple PDN model has been extracted from S parameter measurement.
Output IO	A simplified model of an output buffer has been built from the IBIS file of S12X (see chapter 4 for more information on IBIS file and chapter 8 for more details on S12X models). The model contains only the output buffer. Effects of clamp diodes, pad, package and tracks have been removed to simplify the model.
Oscilloscope	A large band oscilloscope is used to detect a failure during the susceptibility test. The output buffer is sensed by an active probe modeled by a parallel RC. The simulated susceptibility criterion is the voltage across this probe.

Table 3- 6: Details of basic elements of RFI_S12XPowerSupply.sch

III.4.3 Configure the susceptibility simulation

A RFI source is inserted in the schematic to perform a susceptibility simulation. It consists in evaluating the required forward power produced by a RFI source to induce a predefined failure at different frequencies. A transient simulation is used to extract the forward power for a sinusoidal RFI disturbance at a fixed frequency. The amplitude of the RFI voltage is increased linearly during all the simulation, a post-processing is required to detect if a failure appears during the simulation and extract the forward power. The transient simulation is repeated for each frequency of the test.

The first step is the configuration of the susceptibility simulation. Click on the menu “EMC > Susceptibility dBm vs. frequency” or on the icon  . The tool includes two screens: one to control the simulation, and the other to display the extracted susceptibility threshold.

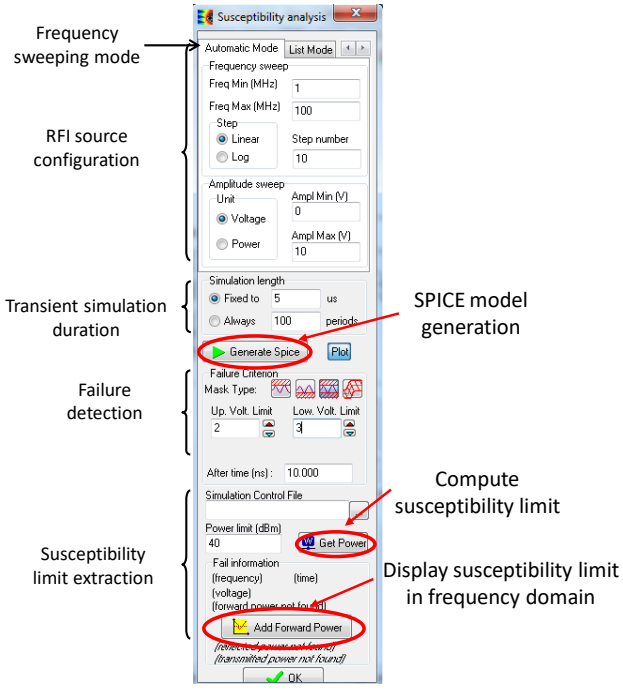


Figure 3- 26: Configuration of the simulation of susceptibility

The disturbance source, susceptibility criterion and transient simulation are configured using this window. The screen used to control the simulation is described in Figure 3- 26. It proposes three tabs dedicated to three simulation modes linked to the RFI frequency sweeping method:

- Manual simulation mode: the user configures a transient simulation at one RFI frequency. The user manually sweeps the frequency.
- Automatic simulation mode (default mode): the user configures N transient simulations for N RFI frequency points. The RFI frequency is swept linearly or logarithmically.
- List simulation mode: this uses the same principle as automatic mode, but the frequency sweeping is defined in a text file.

In this case study, only the automatic mode is considered. The user defines the frequency sweep: here, 20 points ranged logarithmically between 1 and 100 MHz (10 points per decade). Then, the RFI amplitude sweep is configured, either in term of RFI source voltage or forward power. Here, the minimum power is set to 15 dBm while the maximum power is set to 45 dBm. The smaller the amplitude sweep range, the better is the accuracy of the simulation result. Finally, configure the transient simulation duration, defined in absolute time or according to a given number of RFI periods. Set it to 100 RFI periods for every test frequencies. The longer the simulation time, the better is the accuracy of the simulation result.

III.4.4 Run SPICE simulation

In the current version of IC-EMC (version 2.9), the susceptibility simulation is not supported by LTSPICE. In the menu "File > Simulator", verify that WinSPICE has been selected.

In the simulation control screen presented in Figure 3- 26, click on the button “Generate SPICE” to generate the circuit netlist file RFI_S12XPowerSupply.cir and run the transient simulation over the different frequencies. In the menu "File > Simulator > Configurations", depending on the simulator options, the simulation is launched automatically or manually. If the option "Launch simulator manually" is chosen, in WinSPICE, click "File > Open" and select the file RFI_S12XPowerSupply.cir. As the susceptibility simulation is configured for 20 frequency points, the transient simulation is repeated 20 times. The status of each simulation is displayed on WinSPICE interface (Figure 3- 27).

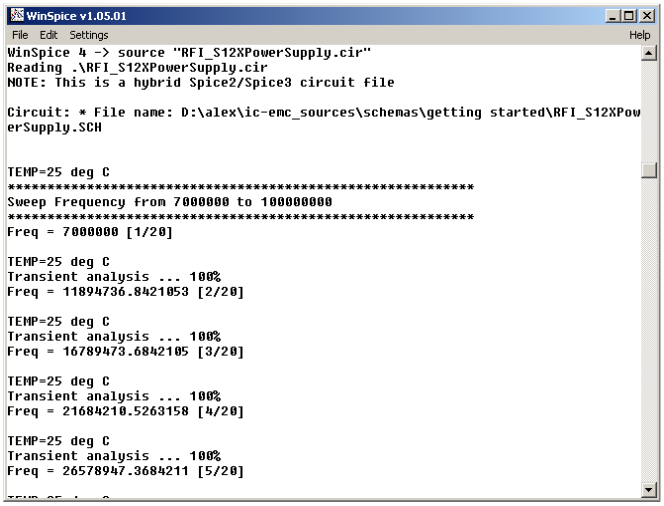


Figure 3- 27: Susceptibility simulation performed by WinSPICE and frequency sweep

III.4.5 Observation of the output signal of the buffer

The susceptibility of the buffer depends on the RF noise coupled on the output buffer. In order to visualize the transient waveform at the output buffer during the RF injection, observe failure and find the failure time, click on the menu "EMC > Voltage vs. time" or on the button . The results of the simulation are recorded in text files with the prefix "sweep_RFI_" followed by the schematic name and ended by the number of frequency sweep. For example, the file " sweep_RFI_RFI_S12XPowerSupply1.txt" is the result of the susceptibility simulation for the first RFI frequency, i.e. 1 MHz. This file contains the transient evolution of the voltage recorded by the voltage probe and the forward and reflected power.

In the "Voltage vs. time" window, click on the button and select the file sweep_RFI_RFI_S12XPowerSupply1.txt. Then select "V(10)" in the list "Signals" to observe the voltage induced at the output buffer. Finally click on the button "Add Simu" to plot this curve. The result is shown in Figure 3- 28. A sine waveform is superimposed to the nominal 5 V voltage delivered by the output buffer. The amplitude of the coupled noise linearly increases with time, since the amplitude of the RF disturbance increases linearly during the simulation. At 27 µs, the amplitude of the coupled RF noise exceeds 1 V so the microcontroller fails.

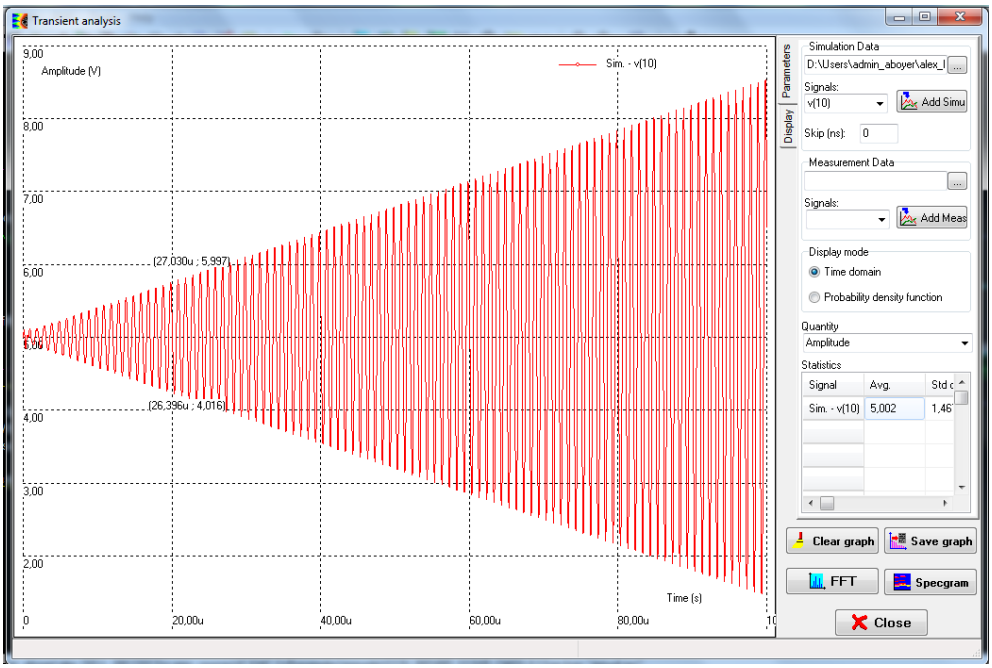


Figure 3- 28: Transient evolution of the voltage induced at the output buffer during the RFI injection at 1 MHz

III.4.6 Susceptibility threshold extraction and comparison with measurement

Return to IC-EMC susceptibility simulation interface or click on “EMC → Susceptibility dBm vs. frequency” or on the icon again. To find all the files associated to transient simulation, a simulation control file *.ctl registers all the result files. If this file does not appear in the field “Simulation control file”, select the file “RFIcontrol_RFI_S12XPowerSupply.ctl”. Then, the susceptibility criterion must be set. The nominal output signal is 5 V and the noise margin is 1 V. Click on the button to set upper and lower limits to the voltage captured by the voltage probe. In the fields "Up Volt. Limit" and "Low Volt. Limit", type 6 and 4 which are the upper and lower limits respectively. Set also the maximum injected power to 45 dBm in the field “Power limit (dBm)” for the frequencies where a failure is not reached during simulation. Finally, click on the button “Get power”. The susceptibility threshold of the microcontroller according to the previous failure criterion is computed for the different RFI frequencies. The susceptibility threshold is expressed in forward power.

At the end of this extraction, click on the button “Add Forward Power” to plot the susceptibility threshold on a Power vs. Frequency graph, as shown in Figure 3- 29. In the tab "Parameters", the X/Y axes settings can be changed. In the tab "Freq.", the numerical values of the forward power are provided. The simulated susceptibility threshold can be saved by clicking on the button "Save".

Click on the button “Add Meas” and select the file “susceptibility_S12X_PDN.tab” to display the measured susceptibility threshold. Figure 3- 29 presents the comparison between measurement and simulation. Despite the gap that can reach up to 6 dB, simulated and measured thresholds follow the same trend and have the same order. This simple model provides an estimation of the susceptibility of the microcontroller rapidly. Increasing the complexity of board and circuit models could improve the accuracy of the simulation.

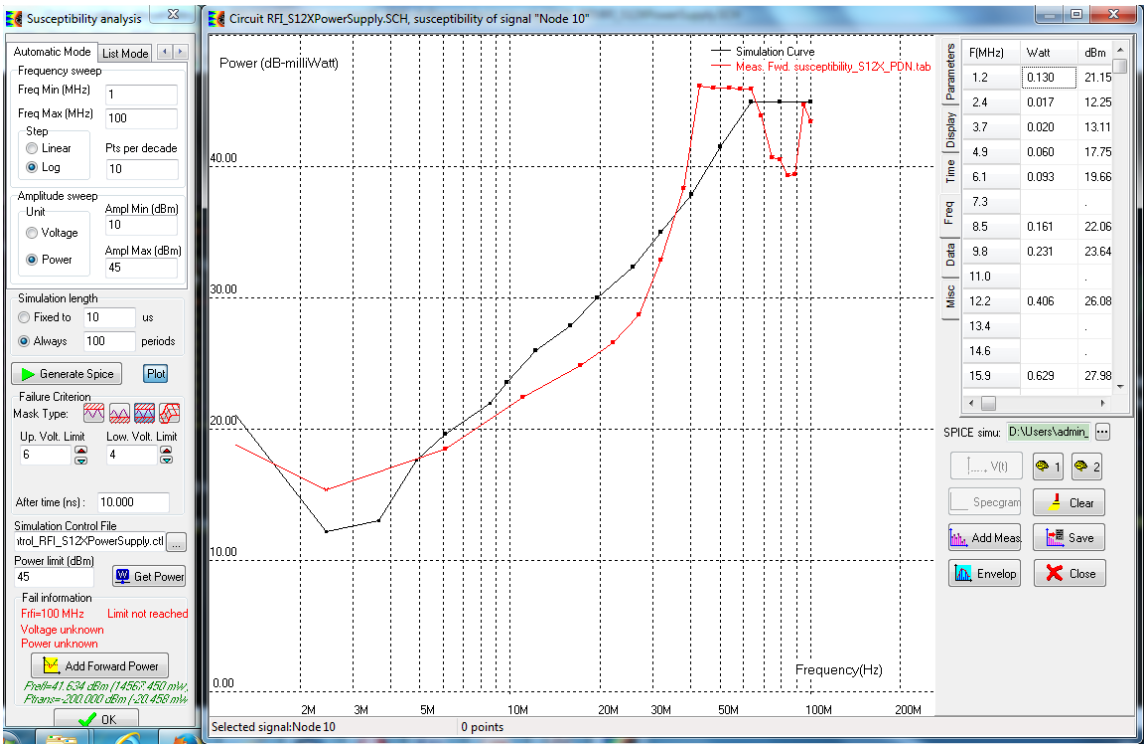


Figure 3- 29: Comparison between measurement and simulation of the susceptibility threshold of the S12X microcontroller (examples\immunity\S12X_RFI\RFI_S12XPowerSupply.sch)

III.5 Load and analyze IBIS file

As more and more attention is focused on the design of very high speed links, for example between processors and memories or display driver and LCD TFT screen, input/output (I/O) models are used for simulating the behavior of signal transport at very high data rate. The accuracy of the simulation relies on the quality of the models, both concerning the ICs and the PCB. Concerning the IC, the input/output buffer specification (IBIS) is recognized by IC manufacturers and users as a worldwide standard for describing IC interfaces to printed circuit boards for signal integrity predictions, without releasing any detailed technological information or confidential aspects of internal structure design [Ibis15]. In this part, we present the IBIS viewer of IC-EMC. With this tool, the user can read the content of an IBIS file, plot the characteristics of the models of the circuit's I/O, reconstruct 2D and 3D views of IC package and evaluate R,L,C stray elements of package interconnects.

III.5.1 Load IBIS file

An IBIS model is formatted as human-readable ASCII text. It is mostly based on extracted tables of generic structural elements. IBIS models are *component-centric*; the IBIS model describes all pins of the physical component with an associated model. Keywords are denoted by square brackets, and a vertical bar serves as the default comment character. The IBIS file mainly contains the following elements:

- **Information and Specification** content starting with a header block [IBIS Ver] and also

presented elsewhere throughout the file

- **Package** information within each of one or more [Component] blocks and under a default [Package] keyword
- **Pin out** information within each of one or more [Component] blocks and under the [Pin] keyword giving pin-specific model references and optional pin-specific package values
- **Model** blocks beginning with one or more [Model] keywords.

The software IC-EMC is able to extract information from IBIS files in a simple way and display it in the IBIS interface. Click on the menu "File > Load Ibis File" or on the button [Ibs] in the command bar, and select the IBIS file “examples\ibis\ Xilinx_Spartan6_LVCMOS33.ibs”, which describe I/O characteristics of the FPGA Spartan6 from Xilinx, mounted in a BGA256 package. The following screen appears (Figure 3- 30). In the left part, the content of the IBIS file is edited and can be read only. In the right part, four tabs appear:

- I/O: the list of the I/Os, the associated models and R, L, C stray elements given by IBIS file are summarized.
- Models: parameters of the I/O models are listed and their characteristics can be plotted (see III.5.2).
- Infos: general information about the IBIS file (version, date, manufacturer, etc), conditions and package are given
- Package: a 2D view of the package is reconstructed by IC-EMC from the pin list and keywords added by the user (see III.5.3).

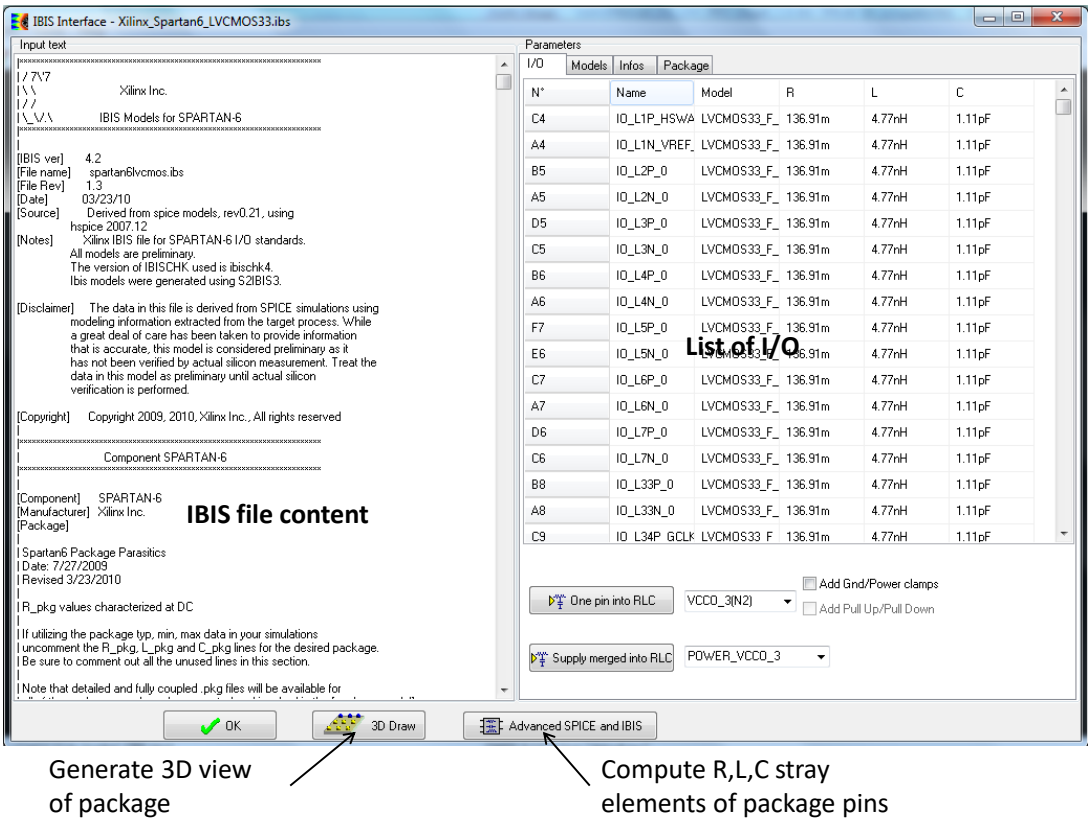


Figure 3- 30: Loading an IBIS file in the IBIS interface (examples\ibis\ Xilinx_Spartan6_LVCMOS33.ibs)

In the "I/O" tab, click the desired input pin in the I/O list, then click the button "One pin into RLC". The input pad is converted into a RLC circuit with on-chip capacitance and clamp, as shown in Figure 3- 31. It consists, from left to right, in an IO symbol with the input name (Here 'IO_L2P_0', the pin B5), the R,L,C parameters for the package (Here LIO_L2P_0, CIO_L2P_0, RIO_L2P_0), and the component input capacitance (Ccomp_IO_L2P_0). Notice the connection to the substrate potential “Vsub”.

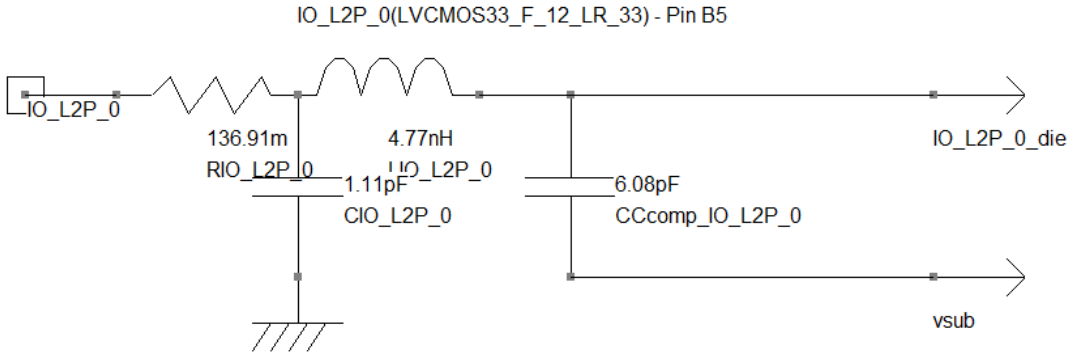


Figure 3- 31: Model of the PT0 pad (examples\ibis\ Xilinx_Spartan6_LVCMOS33.ibs)

III.5.2 Plot I/O characteristics

In an IBIS file, the [Model] block contains the data for electrical simulation of the pin interface. The Model_type sub-parameter classifies the model by types including Input, Output, I/O, 3-state, etc. Static I-V table blocks documented by [Pullup] and [Pulldown] keywords tabulate the transistor drive strengths. In the IBIS window of IC-EMC, the button “Pu” corresponds to the pull-up device of the I/O buffer, and “Pd” to the Pull-down device. The diodes are documented by [Power Clamp] and [Gnd Clamp] I-V tables (“Pc” for Power Clamp, “Gc” for Gnd Clamp). In CMOS technology, clamp diode currents come from P-N junctions. These junctions act as protection circuits from voltage over-stress.

Figure 3- 32 shows the tab "Models" of the IBIS interface. The file " Xilinx_Spartan6_LVCMOS33.ibs" contains six different model instances. Their main characteristics are summarized in the table in the upper part of the tab "Model". Let consider the model called LVCMOS33_F_12_LR33, which is the default model associated to each I/O of the FPGA (actually, each I/O support several I/O standards). It models a push-pull low voltage CMOS output buffer nominally biased under 3.3 V. The terms 'F' and '12' indicate two options of the I/O buffer: '12' is related to the drive (12 mA at V_{OL} = 0.3 V), 'F' is related to the slew rate (fast). It can be seen from the example shown in Figure 3- 32 that pull-up and pull-down I(V) characteristics are available (it is expected since it is a push-pull buffer). A ground clamp I(V) characteristic is available, but the I(V) characteristic of the power clamp is equal to 0. According to the IBIS file, this output buffer has no power clamp protection.

The button "Rw" and "Fw" means "Rising waveform" and "Falling waveform" respectively. Clincking on one of these buttons plots the rising or falling transient profile of the output voltage of the buffer. These V(t) profiles are given after the keywords [Rising Waveform] and [Falling Waveform]. They are used to evaluate the slew rate of the output buffer when it is load by a given load (usually 50 Ω) and fits the command of the I/O in the I/O model.

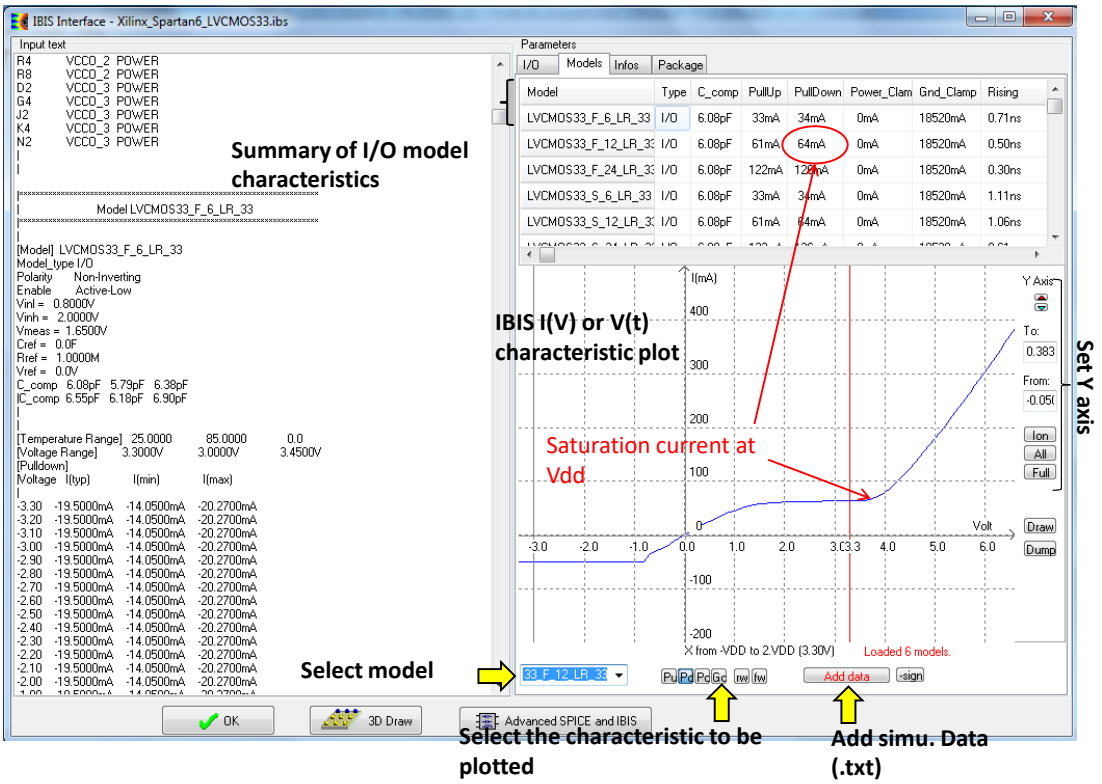


Figure 3- 32: Plotting the I(V) characteristic of the pull-down device of the LVCMOS33_F_12 model (examples\ibis\ Xilinx_Spartan6_LVCMOS33.ibs)

Data provided by IBIS can be used to build an equivalent model of the I/O. Static I(V) simulations can be done to fit the models of pull-down, pull-up or clamp devices. Transient simulations can be performed to verify the rising or falling waveforms of the I/O model. In the IBIS interface, in the tab "Models", user can import SPICE simulation results in .txt file in the IBIS interface by clicking on the button "Add data" and superimpose simulation results with I(V) or V(t) characteristics given by IBIS.

III.5.3 Package viewer

In most cases, accurate R,L,C evaluation of the package leads and bondings is not available in preliminary IBIS files. The purpose of the 2D and 3D-package reconstruction available in IC-EMC is to ease the extraction of package R,L,C elements and gives precise space localization of the package leads and bonding wires. This last point is very useful in EMC analyses, for localization of power supply and ground pins, or or near field radiated emission simulation (see III.8).

III.5.3.1 Hidden Keywords

Some important information is resourced in the IBIS file related to the package and IC physical dimensions. The information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders. The physical dimensions are very important information to rebuild the lead frame structure of the package, together with the bonding structure and access to the die. Table 3- 7 provides a list of the important hidden parameters and associated description added in IBIS file, and used to configure the package viewer in IC-EMC. Figure 3- 33 illustrates the meaning of these geometrical parameters.

Hidden parameter	Description	Example

pack_width	Package width	20.1e-3 m
pack_height	Package height	20.1e-3 m
ic_width	Die witdh	6.55e-3 m
Ic_height	Die height	6.33e-3 m
ic_xstart	Die location in X related to the package	6.73e-3 m
ic_ystart	Die location in Y related to the package	6.84e-3 m
pack_pitch	Package pin pitch	0.5e-3 m
ic_altitude	Die altitude over the ground plane	0.8e-3 m
pack_ball	BGA ball radius	0.25e-6 m

Table 3- 7: Hidden parameters stored in the [package model] section

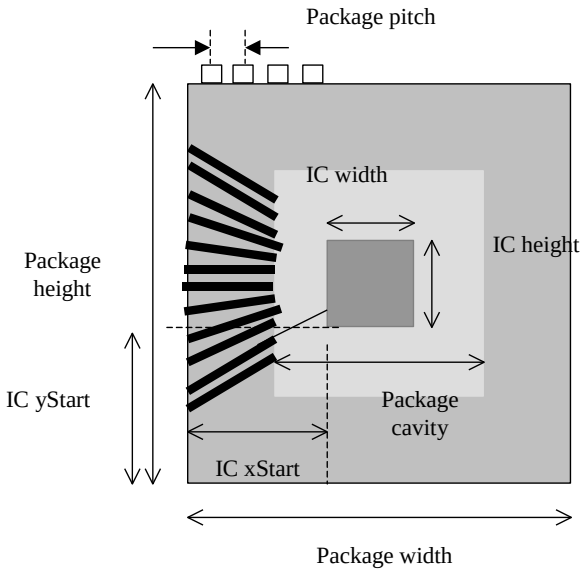


Figure 3- 33 : Main parameters required for an estimation of the package R,L,C model

Different package reconstruction methods exist and depend on the package type. The keyword [Package Model] provides information about the package type.

Keyword	**Package types and variants**	**IBIS example file**
[Package Model] bga	Ball Grid Array (BGA)	infineon_tc1796.ibs, Xilinx_Spartan6_LVCMOS33.ibs, virtexIIXC2V1500.ibs, prometheus_mmm6030_v2.ibs, bga64.ibs, mpc5534-324.ibs
[Package Model] sop	Small Outline Package (SOP)	ahct04.ibs
[Package Model] soic	Small Outline Integrated Circuit (SOIC)	l4949_v4.ibs
[Package Model] qfp	Quad Flat Package (QFP)	Cesame_v14.ibs S12x_v2.ibs
[Package Model] dil	Dual in line (DIL)	ds90lv049.ibs, NCP5603_v4.ibs

Table 3- 8: Examples of package declaration in the ibis file (IBIS files available in examples\ibis)

III.5.3.2 2D Package Viewer

The need for reconstructing the 2D aspect of the package is justified by the need to locate pins (especially power supply and ground pins), and to provide accurate space coordinates of lead and bonding wires for near-field scan prediction. The external aspect of the IC with pin placement may be displayed by a click on the tab “Package” (Figure 3- 34).

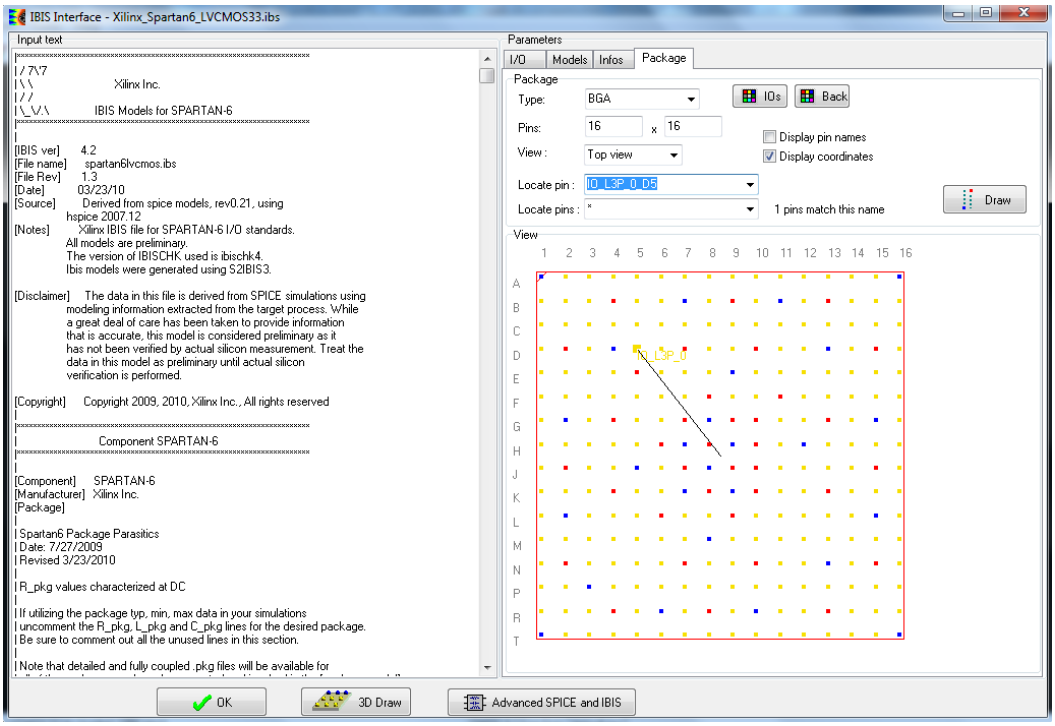


Figure 3- 34: Package viewer (examples\ibis\ Xilinx_Spartan6_LVCMOS33.ibs)

The yellow color corresponds to general purpose I/Os, the VDD supply pins are drawn in red, and the VSS pins in blue. Non-connected pins are drawn in gray. This 2D view gives details on the supply structure. It is also used by IC-EMC to compute the approximate position of a package lead. Considering the pin “IO_L3P_0_D5” selected in the list "Locate pin", an [X,Y] position is assigned to the lead which appears as a black line in Figure 3- 34. A group of pins (e.g. power supply pins) can also be located by selecting this group in the list "Locate pins".

III.5.3.3 3D package Viewer

The 3D-viewer is a visual assistant but do not include specific EMC features. The need for reconstructing the 3D aspect of a package is justified by the two following items:

- Compute accurate values for R,L,C of the package based on the physical dimensions of leads and bonding, if not provided in IBIS
- Provide accurate space coordinates for lead and bonding wires for near-field scan prediction

The 3D package viewer gives a three-dimensional interactive view of the package. To create the 3D view, from the IBIS interface, click on the button "3D Draw". An example of 3D view of the BGA package of the Spartan 6 FPGA is given in Figure 3- 35. You may change the viewer’s position thanks to cursors X,Y and Z. The Z cursor serves as a zoom. The light position may be changed. The bonding, upper part of the package and the IC may be removed from the drawing. Finally, you may see a particular pin in the pin lists "Locate" in the lower corner of the user’s menu. The demo button makes an automatic rotation of the object, and the “close” button closes the window.

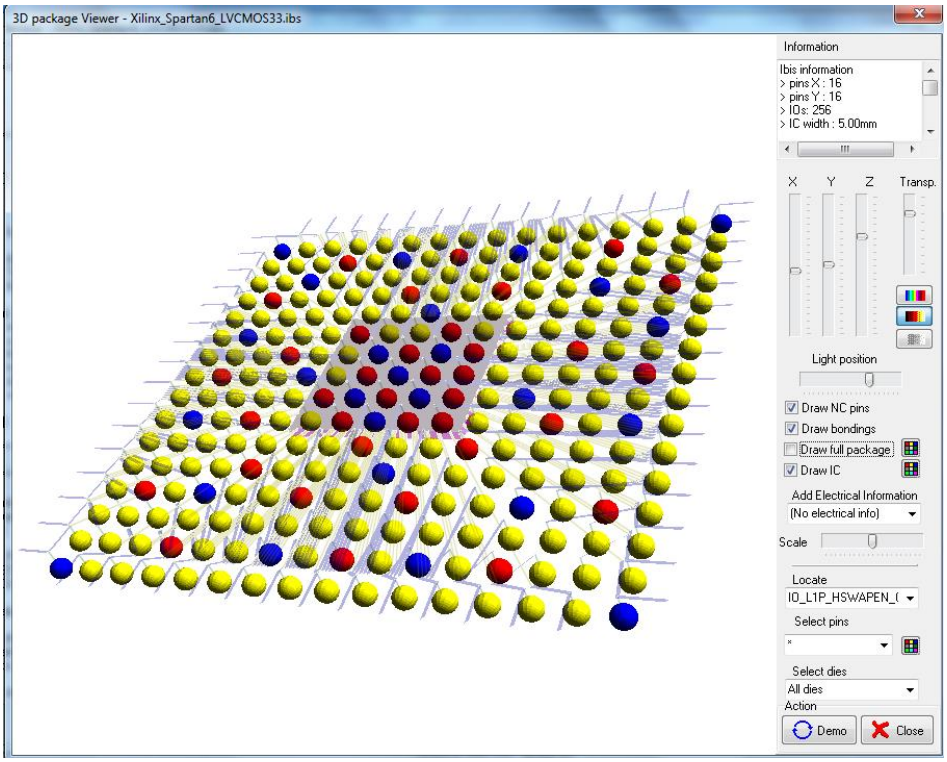


Figure 3- 35 : 3D view of a BGA package (case study/tricore/infineon_tc1796_v2.ibs)

III.5.4 Package modeling

Refer to the example presented in III.8.3.1.

III.6 Transient signal analysis

This example aims at presenting the resources to analyze time-domain properties of signals. In this short case study, a complex signal is generated and its characteristics are studied. The following sections describe the different steps used to generate the signal and extract its characteristics.

III.6.1 Signal generation

In this example, a chirp modulated signal is considered. This type of signal is used in radar communications, but also in spread spectrum modulation (e.g. LoRa modulation). A chirp is a pseudo-periodic signal which frequency-modulated around a central or carrier frequency. The particularity is that the instantaneous frequency of the signal increases or decreases with time. In this example, we consider a linear chirp, i.e. the instantaneous frequency

changes with time linearly according to a constant parameter μ_0 called chirp rate. A general expression of its waveform is defined by the following equation:

$$s(t) = A\cos\theta(t) = A\cos\left[2\pi\left(F_C - \frac{B}{2}\right)t + \pi\mu_0 t^2\right], \quad t \in [0; T_{chirp}] \qquad \textit{Equ. III-5}$$

where F_C is the central frequency, B is the bandwidth occupied by the signal and T_{chirp} the duration of the chirp. The chirp rate is given by the equation below. If μ0 is positive, the instantaneous frequency increases with time, otherwise it decreases.

$$\mu_0 = \pm\frac{B}{T_{chirp}} \qquad \textit{Equ. III-6}$$

The instantaneous frequency of such a signal is given by the equation below. It shows that the instantaneous frequency is linearly dependent of time.

$$F_{inst} = \frac{1}{2\pi}\frac{d\theta(t)}{dt} = F_C - \frac{B}{2} + \mu_0 t \qquad \textit{Equ. III-7}$$

In digital chirp-based modulation, the transmitted is composed of a series of chirp. Information is encoded either by sign of the chirp rate, or by a frequency offset added to the instantaneous frequency (e.g. LoRa modulation).

IC-EMC proposes a tool dedicated to the generation of complex waveforms that can be imported in SPICE schematics. Click on "Tools > PWL Source Generator" to open the window of signal generation. This tool aims at generating the time-domain profile of signals in SPICE compatible Piece-Wise Linear (PWL) format. The profile is defined by a series of pairs of value (Ti, Vi) where the value of the source is Vi (in Volts or Amps) at time=Ti. At intermediate values of time, the value of the source is interpolated. This profile can be saved in a text file and then imported in a SPICE netlist to describe the transient waveform of a voltage or current generator.

The window shown in Figure 3- 36 opens. In the area "Select the mathematical operation", select "Linear up/down chirp". In the central part of the screen, the parameters of the signal can be modified:

- Samples and step: the number of pairs of value (Ti, Vi) of the PWL signal and the time step between two pairs
- Frequency F_C: the nominal frequency of the chirp signal
- Amplitude A and offset: the amplitude and the offset of the chirp signal
- Chirp rate μ_0: the linear increase or decrease rate of the instantaneous frequency of the chirp
- Chirp duration T_{chirp}: the duration of one chirp

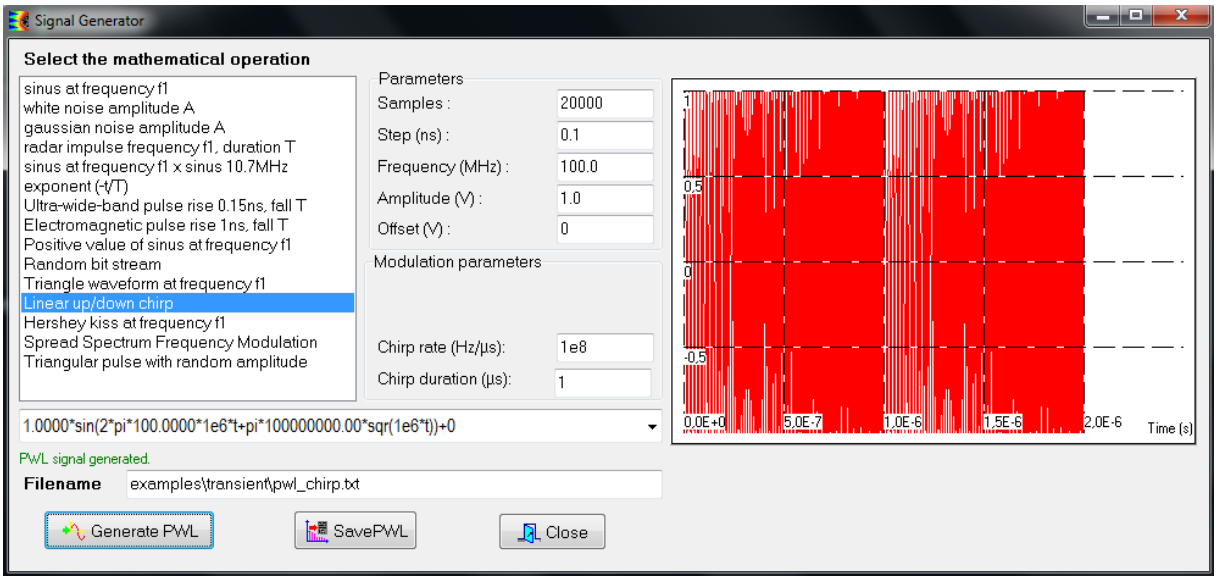


Figure 3- 36 : PWL signal generator window ("Tools > PWL Source Generator")

Here, we select the parameters shown in Figure 3- 36: the central frequency is 100 MHz, the chirp rate is 100 MHz/µs and one chirp lasts 1 µs. Thus, the bandwidth occupied by the chirp signal should be 100 MHz centered around 100 MHz. Here, the tool will generate 20000 points separated by 0.1 ns, so the total duration of the signal will be 2 µs, i.e. two chirp duration.

Click on the button "Generate PWL" to display the waveform of the signal on the right part of the window. Click on the button "Save PWL" to save the PWL signal in a .txt file. The file pwl_chirp.txt has been saved in the directory "\examples\transient\". Click on the button "Close" to quit the window.

III.6.2 Create the model

Create a new schematic. Place a voltage source, a ground reference and a voltage probe, and save it. Double-click on the voltage symbol to edit its properties. Select Piece-Wise Linear and import the text file "\examples\transient\pwl_chirp.txt" by clicking on the button ... . Click on the button "OK" to validate and close the window.

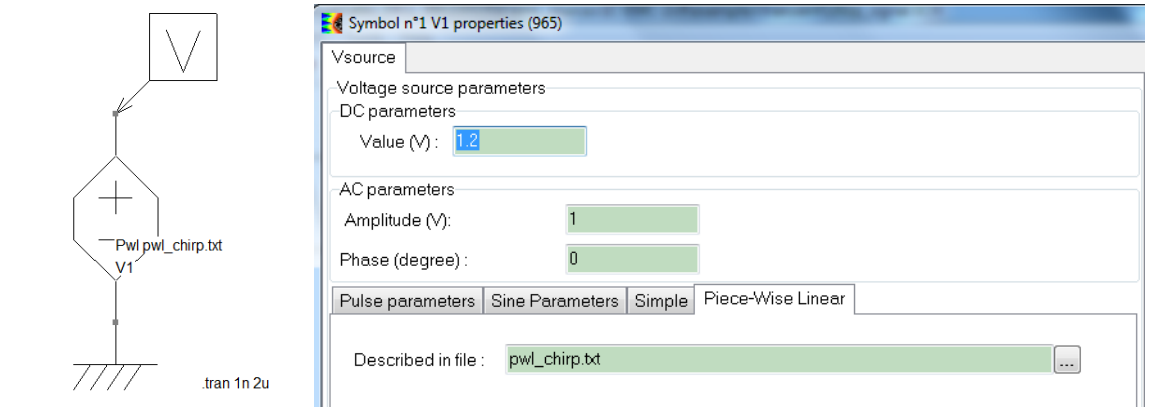


Figure 3- 37 : Model for simulation of chirp signal (\examples\transient\chirp_signal.sch) and PWL voltage source configuration

Configure the transient simulation : click on "Insert > Insert Analysis Line" and set a stop time of 10 µs and a step time of 1 ns.

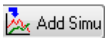
III.6.3 Run SPICE simulation

Select LTSPICE as simulation in "File > Simulator". In "File > Simulator > Configurations", you can select "Batch mode" to launch LTSPICE simulation automatically each time the SPICE netlist is updated. Click on the button  to generate the SPICE netlist and launch the SPICE simulation. At the end of the simulation, the result is recorded in a .raw file (chirp_signal.raw).

III.6.4 Observe the time-domain waveform

Open the "Voltage vs. time" window by clicking in the menu "EMC > Voltage vs. time" or on the button  in the command bar. The window shown in Figure 3- 38 opens, showing the transient evolution of the chirp signal. Two tabs appears on the right side of the screen:

- Parameters: import simulation and measurement results, select signals to be displayed and display mode.
- Display: X/Y axes settings, show/hide curves, memorize curves

If the curve is not plotted, you can import the simulation result (\examples\transient\chirp_signal.raw) by clicking on the button  in "Simulation Data" part. The signals (voltage and current) recorded in the .raw file appear in the list "Signals". Select the signal 'v(1)' and click on the button 

to plot the chirp signal. The X and Y axes can be set with the commands proposed in the tab "Display". Zoom and curve memorization commands are also available.

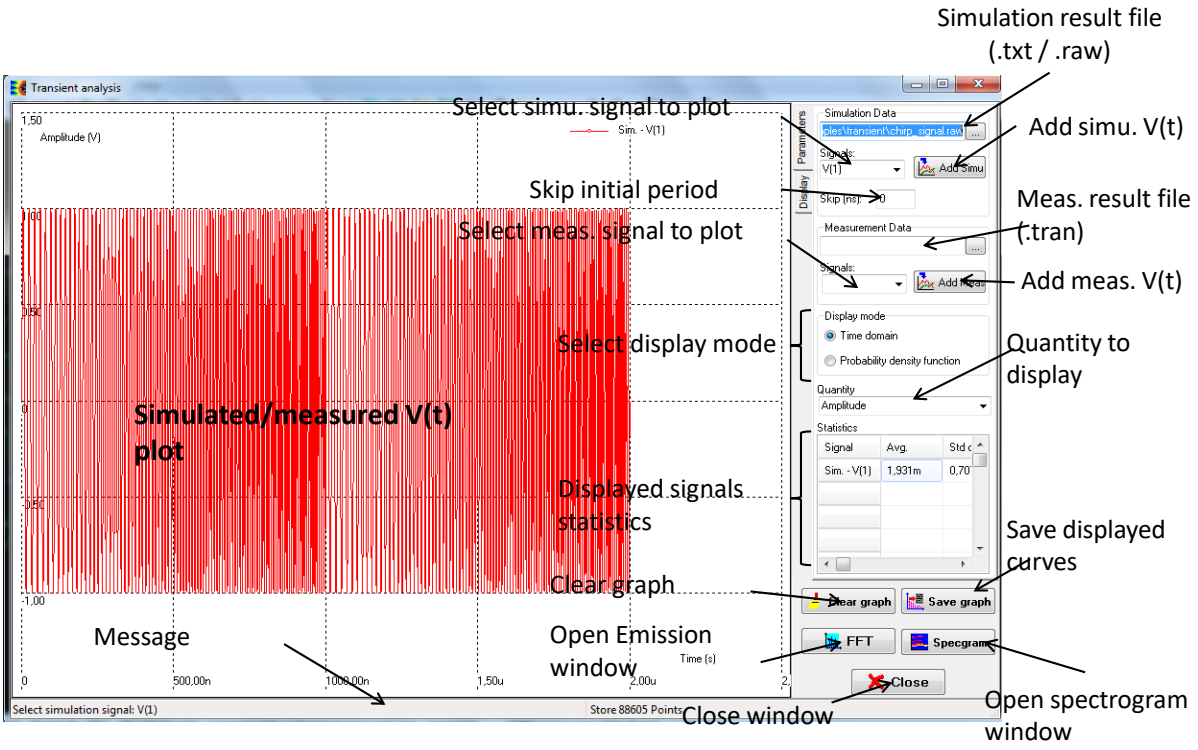


Figure 3- 38 : Simulated waveform of the chirp signal (\examples\transient\chirp_signal.sch)

Several characteristics or quantities of signals can be displayed, according to the selection done in "Quantity" field:

- Amplitude: this is the default displayed quantity
- Rise /fall time: 10%-90% rise and fall times
- Period and Frequency
- Duty cycle
- Jitter: phase jitter, period jitter or cycle-to-cyle (C2C) jitter

These quantities can be displayed according to two different modes:

- "Time domain" mode: the evolution of the selected quantity is plotted in time domain
- "Probability density function" mode: an histogram showing the probability of occurrence of the values taken by the selected quantity is plotted

III.6.5 Analysis of the instantaneous frequency of the signal

Figure 3- 38 shows the transient evolution of the signal. Clearly, the signal is a sine wave whose frequency increases regularly during 5 µs. However, the exact evolution of the signal frequency is difficult to read accurately. To observe it, select "Frequency" in the "Quantity" field. The result is shown in Figure 3- 39 and confirms that the instantaneous frequency of the signal increases linearly from 5 MHz to 15 MHz for 5 µs periodically. The statistics of the instantaneous frequency can be found in the first row of the table "Statistics": the average frequency is about 10 MHz, while the minimum and maximum frequencies are nearly 50 and

150 MHz. The statistics is determined from 198 occurrences of signal periods. This figure is given in the last column of the table "Statistics".

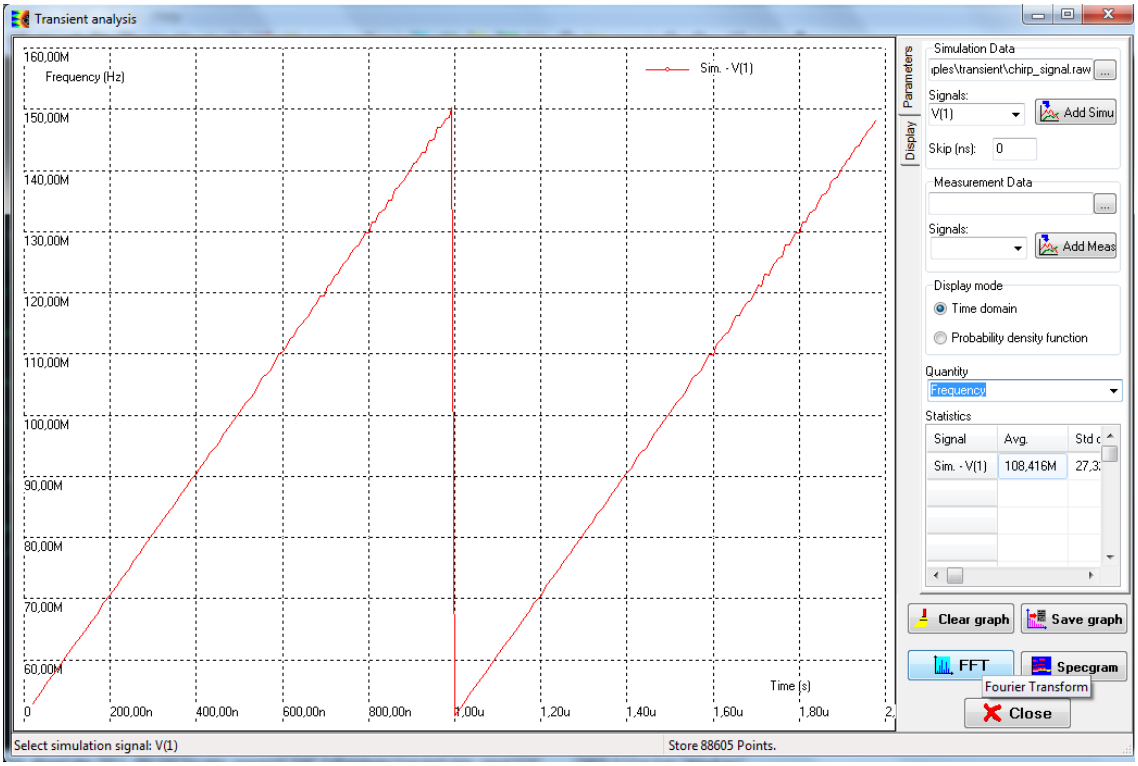


Figure 3- 39 : Evolution of the instantaneous frequency of the simulated chirp signal (\examples\transient\chirp_signal.sch)

The distribution of the instantaneous frequency taken by the chirp signal can be plotted if you select the box "Probability density function" in the field "Display mode", as shown in Figure 3-40. The constructed histogram is centered around 100 MHz and shows the distribution of the frequency of the occurrence of chirp signal period.

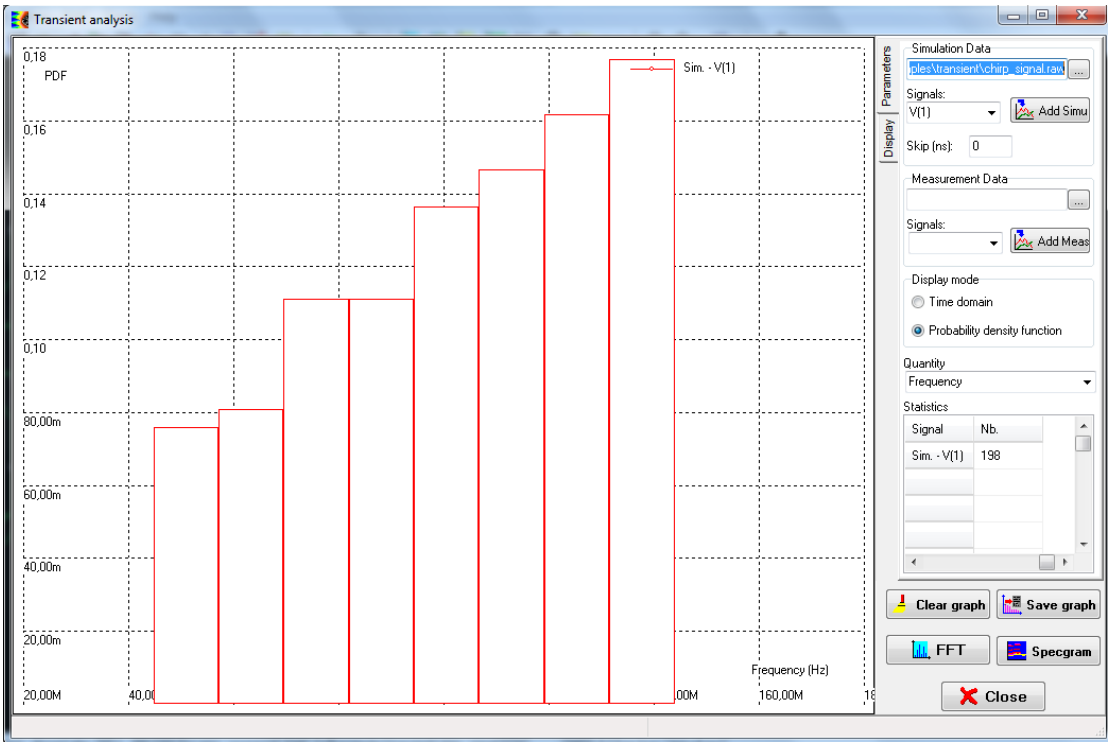


Figure 3- 40 : Statistical distribution of the instantaneous frequency of the simulated chirp signal (\examples\transient\chirp_signal.sch)

III.6.6 Spectrogram

From the "Voltage vs. time" window, frequency analysis based on FFT can be done. Clicking on the button FFT opens the 'Emission Window' as described in III.1. A FFT of the full signal is computed, so that the evolution of the instantaneous frequency of the chirp signal cannot be displayed. A more interesting analysis of this signal is provided by a short-term FFT (SFFT) which can be computed with the tool Spectrogram. It can be opened with the button Specgram or from the menu "Tools > Spectrogram". This tool display a representation of the signal in both time and frequency domains, as shown in Figure 3- 41. The amplitude of the signal is plotted according to a color code in a X-Y surface, where X is the time axis and Y the frequency axis. You can change the maximum displayed frequency by selecting the option "Max. Freq. (MHz)". An parameter of the SFFT is the FFT resolution N_{reso}. SFFT consists in performing successive FFT on M_B time block of N_{reso} points. The time resolution of the SFFT is the duration of one time block. In this example, the maximum frequency is set to 500 MHz and the FFT resolution is set to N_{reso} = 1024 points. As the sampling period T_E is 0.1 ns, the maximum frequency of the FFT is $F_E = 1/T_E$ = 5 GHz. The duration of one time block, i.e. the time resolution is thus $(N_{reso}-1)xTE$ = 102.3 ns. We can conclude that the lower the FFT resolution, the better the time resolution. However, reducing the FFT resolution degrades the frequency resolution. The frequency resolution dF is inversely proportional to the duration of one time block: $dF = F_E/(N_{reso}-1)$ = 4.89 MHz. The lower the FFT resolution, the worst the frequency resolution.

In the example shown in Figure 3- 41, we can observe that the frequency increases linearly between 50 to 150 MHz for 1 µs.

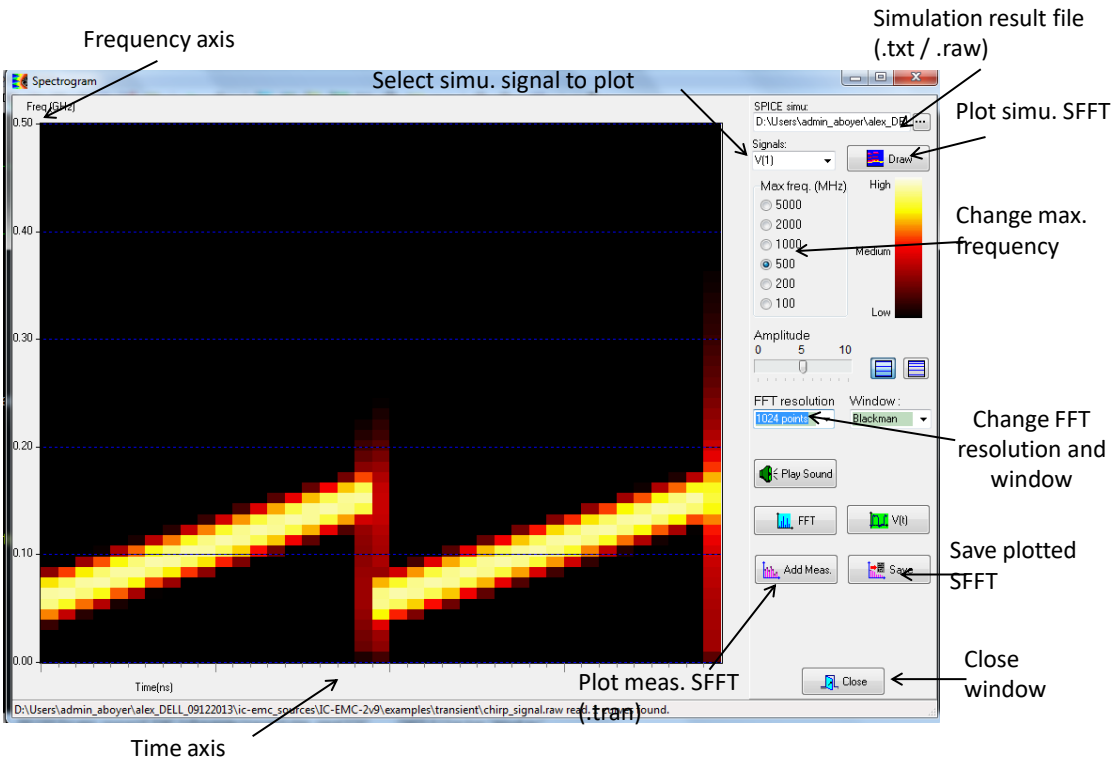


Figure 3- 41 : Spectrogram or SFFT of the simulated chirp signal (\examples\transient\chirp_signal.sch)

III.7 Plot an eye diagram

Eye diagram is a commonly used tool to assess the quality or the integrity of high-speed digital signals (Ethernet, USB3, HDMI, PCIe, etc). The transmission through transmission lines may distort the signal waveform because of impedance mismatch, attenuation, crosstalk with neighbour lines, simultaneous switching noise, etc. The amplitude and time distortion of the signal may lead to bit misinterpretation by the receiver. Eye diagram helps designers to view the signal impairments more easily, detect bandwidth limitation or the presence of excessive overshoots.

The following sections aims at presenting how to plot the eye diagram of a digital signal and analyse its integrity. The proposed example addresses a link between two SSTL15 I/O buffers interconnected through a microstrip line. I/O buffers are described by macromodels built from IBIS file information.

III.7.1 Eye diagram

Figure 3- 42 describes the principle of the construction of the eye diagram of high-speed digital signal. It is essential to underline that eye diagram measurements concern only digital synchronous signals. Although eye diagrams apply for 2 or more level logic signal, only binary signals are considered in IC-EMC and in the following sections.

Let consider the transmission of a binary signal between a digital transmitter (TX) and a digital receiver (RX) through a series of interconnects. The data transfer is synchronized on the data clock rate F_{CLK}. The construction of an eye diagram is based on a high bandwidth sampling of the signal data stream and an accumulation of the measured samples in order to superimpose all the states of the signal ('1' and '0' levels, transitions from '0' to '1' or '1' to '0'). To obtain a stable picture, this sampling must be triggered on a clock which is synchronous with the captured digital signals. Thus the sampling is triggered at the signal binary data rate. Here, this clock signal is called the data clock.

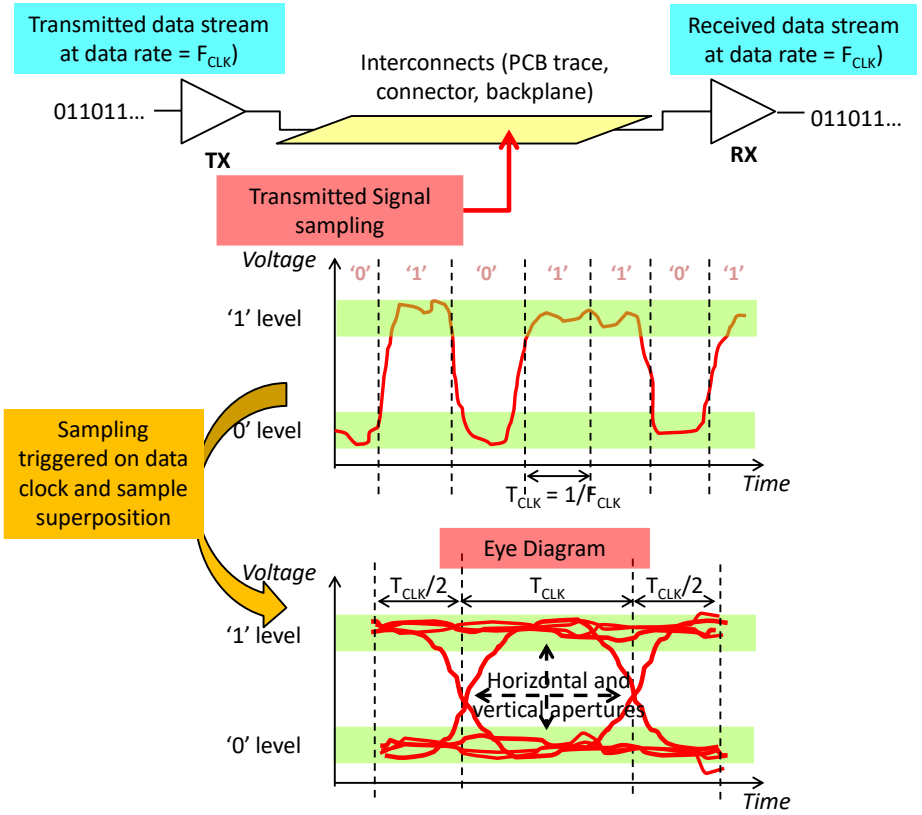


Figure 3- 42: Principle of the construction of an eye diagram

The display of an eye diagram is usually normalized for two clock periods and is centered on one bit period in order to capture the rising and falling transitions of the signal. The superposition of all the samples forms an eye, which gives the name to this diagram. A properly constructed eye diagram should contain every possible bit sequence, from simple '0' -'1' or '1' - '0' transitions to long sequences of '0' or '1'.

Eye diagram provides an easy way to control the quality of the signal. The more open the eye is (horizontal and vertical aperture), the lower the likelihood that the receiver misinterprets the incoming signal. Noise and time jitter introduce some closure of the eye opening and increases the risk to confuse binary symbols (bit error rate (BER)). Moreover, any transitions that pass through the center of the eye opening may cause bit errors.

However, eye diagram is not only a graphical representation to make qualitative assessments of signal integrity. Several indicators can be extracted to quantify the signal integrity. Figure 3- 43 describes the signal integrity indicators extracted from the eye diagram's tool of IC-EMC. There are two types of indicators:

- Amplitude or vertical indicators:

    1. Level '0' and Level '1': average value of the '0' and '1' levels in the 40-60 % region

2. Eye amplitude: difference between Level '1' and Level '0'
3. Eye height or vertical aperture = (Level '1'-3xσ_1) - (Level '0'-3xσ_0), where 3xσ_1 and σ_0 are the standard deviations of sample distribution around Level '1' and Level '0' in the 40-60% region. It is an indicator of the vertical eye opening.
4. Eye crossing level: the amplitude of the transition crossing points.
5. Eye crossing percentage = 100x(Eye crossing level - Level '0')/(Level '1' - Level '0'). It gives an indication of pulse symmetry.
6. Signal to Noise Ratio (SNR): ratio of the desired signal level (eye amplitude) to the level of noise plus distortion. SNR = (Level '1' - Level '0')/(σ_1+ σ_0). The higher the SNR is, the lower the amplitude distortion.

- Time or horizontal indicators:

7. Jitter: the time deviation from the ideal timing of a bit event (i.e. a transition) and its actual realization. Jitter is computed as the time variance of the rising and falling transitions at the crossing points. In IC-EMC, only the peak-to-peak jitter is computed.
8. Eye width or horizontal aperture = (Right cross. point time - 3xσ_{Tr}) + (Left cross. point time - 3xσ_{Tl}), where σ_{Tr} and σ_{Tl} are the time variances of the rising and falling transitions at crossing points right and left. It is an indicator of the horizontal eye opening.
9. Rise and fall times: 10 to 90 % rise or fall times.

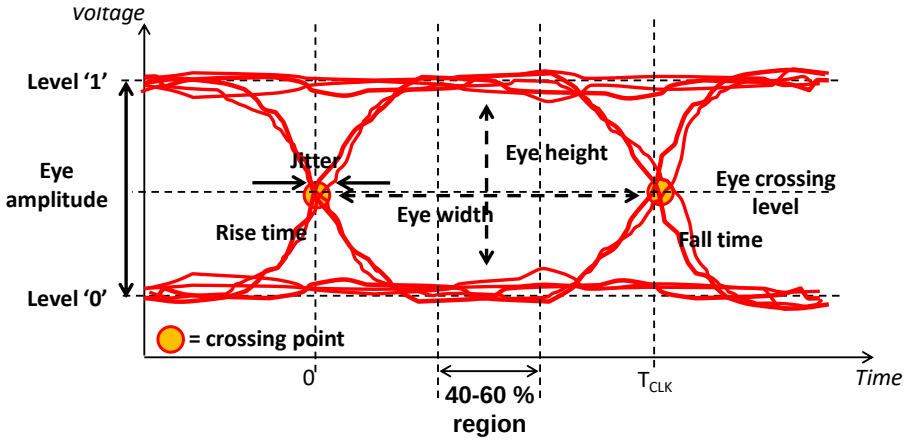


Figure 3- 43: Signal integrity indicators extracted from eye diagram

III.7.2 Load the example: DDR3 memory link

In order to illustrate the creation of an eye diagram, we consider a DDR3 memory link as example. Open the example in "examples\transient\ DDR3_link_400MHz.sch" by clicking on "File > Open". In the next part, we will modify this schematic diagram to plot the eye diagram.

The schematic presented in Figure 3- 44 models a connection between a DDR3 driver (DDR3 TX) and a DDR3 receiver (DDR3 RX) through a microstrip line designed on a PCB. DDR3 or DDDR3 SDRAM is actually a type of synchronous dynamic random access memory. The term DDR3 is used to talk about the interface. The schematic models a link between a microprocessor and an external DDR3 SDRAM memory for example.

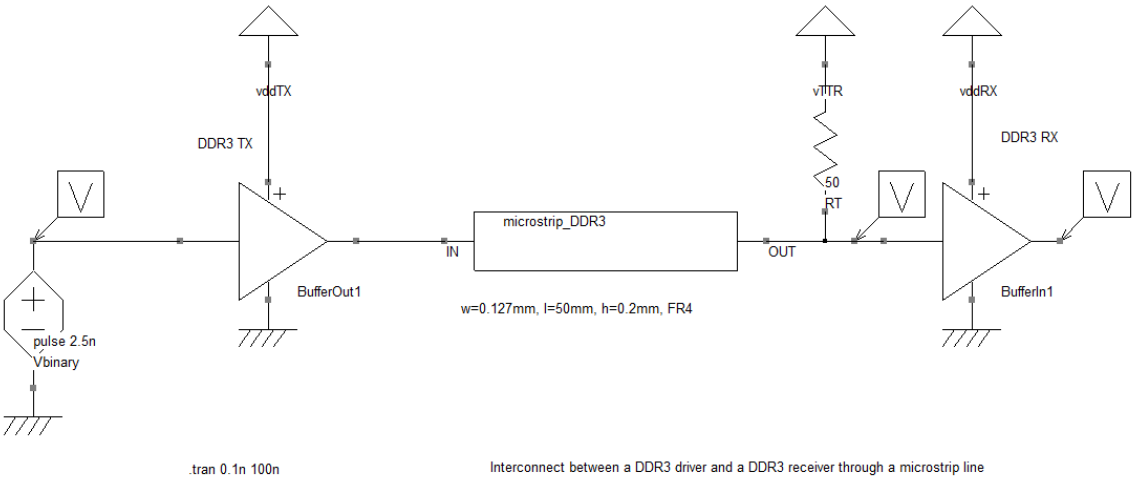


Figure 3- 44: Model of a DDR3 memory link (\examples\transient\DDR3_link_400MHz.sch)

The microstrip line model is included in the subcircuit "microstrip_DDR3.sym". It was created based on the geometrical dimensions of the line by the tool "Tools > Interconnect parameters" (refer to III.9.1). The microstrip line is routed on a multilayer FR4 PCB. The dimensions of the line are:

- width = 0.127 mm
- height to the reference plane = 0.2 mm
- copper thickness = 35 µm
- length = 50 mm

The characteristic impedance computed by "Tools > Interconnect parameters" is nearly 80 Ω. The DDR3 driver and receiver comply with the SSTL15 standard specified by JEDEC Standard JESD79-3. It is a general-purpose 1.5V memory bus standard, which requires a termination voltage of 0.75V and a termination resistor of 50 Ω. Output buffers are push-pull types. The driver and receiver have been modeled from information contained in IBIS file. In this example, the I/O buffer's models have been derived from IBIS file of a Spartan 6 FPGA available in "\examples\ibis\Xilinx_Spartan6_SSTL15.ibs". Macromodels have been constructed to reproduce the characteristics given in IBIS file. The construction of such a model is not addressed in this part. The instance of the driver is an "Output buffer", its symbol can be found in the symbol palette  . The macromodel associated to the buffer is given by the subcircuit "\examples\ibis\IO_models\SSTL15_II_LR33_v3.sym". The "Output buffer" symbol has 4 terminals: power supply references VDD and VSS, a logic input (0-1 V signal) and the physical output. The instance of the receiver is an "Input buffer", its symbol can be found in the symbol palette  . The macromodel associated to the buffer is given by the subcircuit "\examples\ibis\IO_models\ SSTL15_IN_Typ_v2 .sym". The "Input buffer" symbol has also 4 terminals: power supply references VDD and VSS, the physical input and a logic output (0-1 V signal).

If you double-click on the driver or the receiver, the properties of the symbols can be edited, as shown in Figure 3- 45. The field "I/O model" specified the subcircuit file containing the macromodel of the I/O buffer. The fields "Resistance", "Inductance", "Capacitance" in the "Package" part define the R, L, C stray elements associated to the package input or output pin. For "Input buffer" symbol, the properties "High threshold" and "Low threshold" specify the logical voltage threshold of the input buffer.

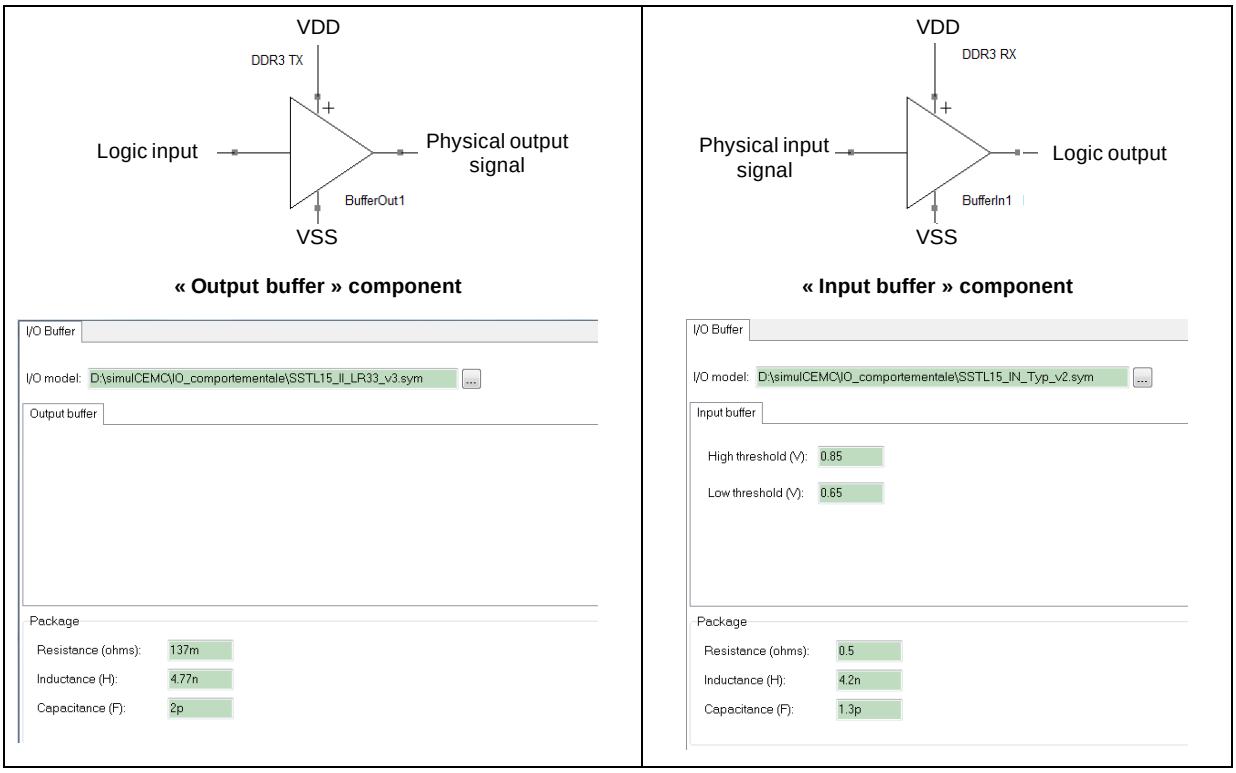


Figure 3- 45: Properties of DDR3 driver (left) and receiver (right) (\examples\transient\ DDR3_link_400MHz.sch)

The resistor RT is a termination resistor which is connected to a 0.75 V termination voltage. The logic input of the DDR3 driver is driven by a 5 ns periodic square waveform signal. It simulates a 400 Mbits/s logic signal with regular '0'-'1' transitions. In this example, the transient profile of the signal delivered by DDR3 driver is simulated, thanks to the command line ".tran 0.1n 100n". Three voltage probes have been placed: on the logic input of DDR3 TX (node 4), at the output of the microstrip line (node 1) and at the logic output of DDR3 RX (node 6).

In "File > Simulator", select WinSPICE and click on  to generate the netlist and launch the simulation. At the end of the simulation, click on the button  to observe the signals. In the tab "Parameters", select the three signal to display and click on the button "Add Simu". In the tab "Display", you can adjust the scale to zoom on one or two binary periods, as shown in Figure 3- 46. The blue and the green curves show the logic signal at the input of DDR3 TX and DDR3 RX respectively. There is a delay of nearly 1.6 ns between both signals due to the switching time of the SSTL15 output and input buffers and the transmission time through the microstrip line. The red curve shows the simulated physical signal at the input of DDR3 RX. The waveform of this signal has been affected by the characteristics of the line, the mismatch between the line impedance and the termination impedance and the R,L,C stray elements of DDR3 TX and DDR3 RX package. A more appropriate representation to analyse the effect of the physical transmission to the signal integrity is offered by the eye diagram.

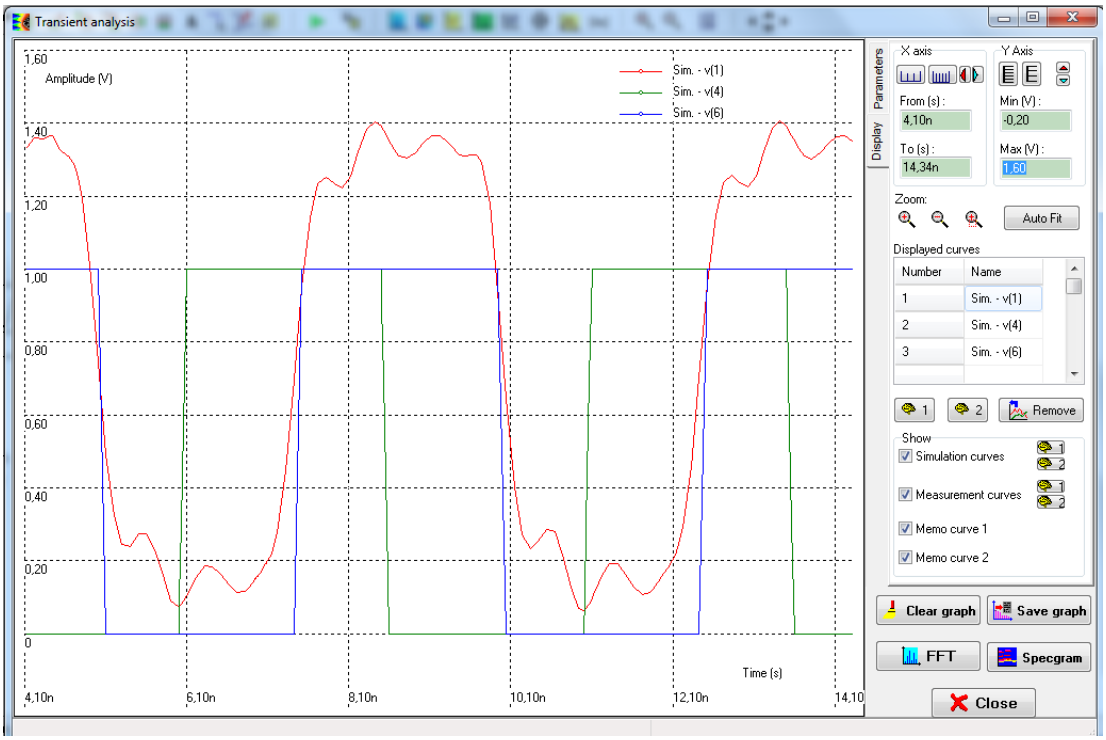
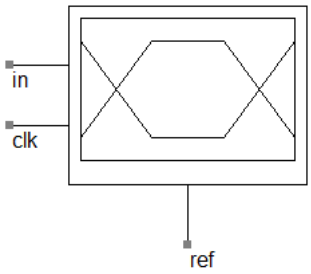


Figure 3- 46: Transient simulation of a DDR3 memory link (\examples\transient\ DDR3_link_400MHz.sch)

III.7.3 Eye diagram probe

An eye diagram probe must be placed on the schematic in order to plot an eye diagram representation after a transient simulation. The eye diagram probe is found in the symbol palette  . In this part, the previous schematic will be modified to set-up the simulation for eye diagram plotting.

Save the previous schematic as " DDR3_link_400MHz_eye_diagram.sch" with "File > Save as". Place an eye diagram probe on the schematic. This component has three terminals:



- in: connect the signal that you want to analyse
- clk: connect the data clock on this terminal
- ref: connect the ground

Terminal "in" is connected to the output of the microstrip line. Terminal "ref" is connected to the ground. In the previous schematic, no data clock source were present. We must create a clock source which is synchronized on the binary signal transmitted by DDR3 TX. This source must produce a rising transition at each binary transition of the signal connected on terminal "in". Thus, a voltage source called "V_data_clock" is inserted on the schematic, with the properties shown below. The period of the data clock source is set to the binary period, i.e. 2.5 ns in order to be synchronous with the transmitted binary signal (400 Mbits/s). A delay of 1.6 ns (field "TD") is introduced to compensate the delay between the signal transmitted through the microstrip line and the data clock.

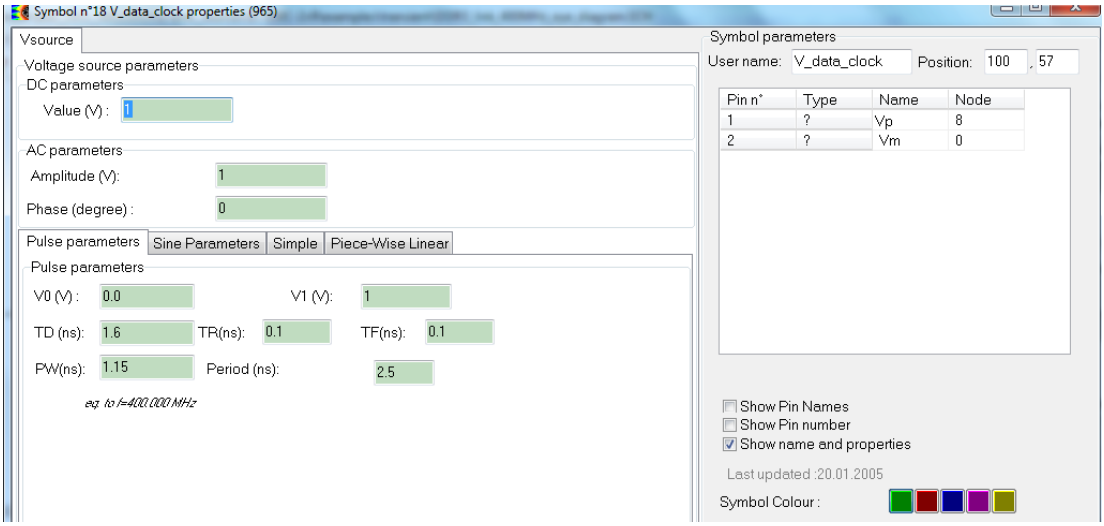


Figure 3- 47: Prepare the simulation for eye diagram plotting - set the data clock source (\examples\transient\ DDR3_link_400MHz_eye_diagram.sch)

Only one active eye diagram probe should be placed on the schematic. The other voltage probes can remain active. The schematic should look like the diagram shown in Figure 3- 49.

III.7.4 PRBS source

The model is not completely achieved to perform an eye diagram analysis. The source connected to the input of DDR3 TX produces a regular logic sequence '010101…". As explained before, a properly constructed eye diagram should contain every possible bit sequence. A commonly used source for this purpose is called Pseudo-Random Binary Sequence generator. It can produce a synchronous logic signal whose logic state change randomly at each clock period. Such a source can be constructed in IC-EMC by generating a Piece-Wise Linear (PWL) signal. Click on the menu "Tools > PWL Source Generator" and select "Random bit stream (PRBS)" in the field "Select the mathematical operation". Set the parameters shown in Figure 3- 48.

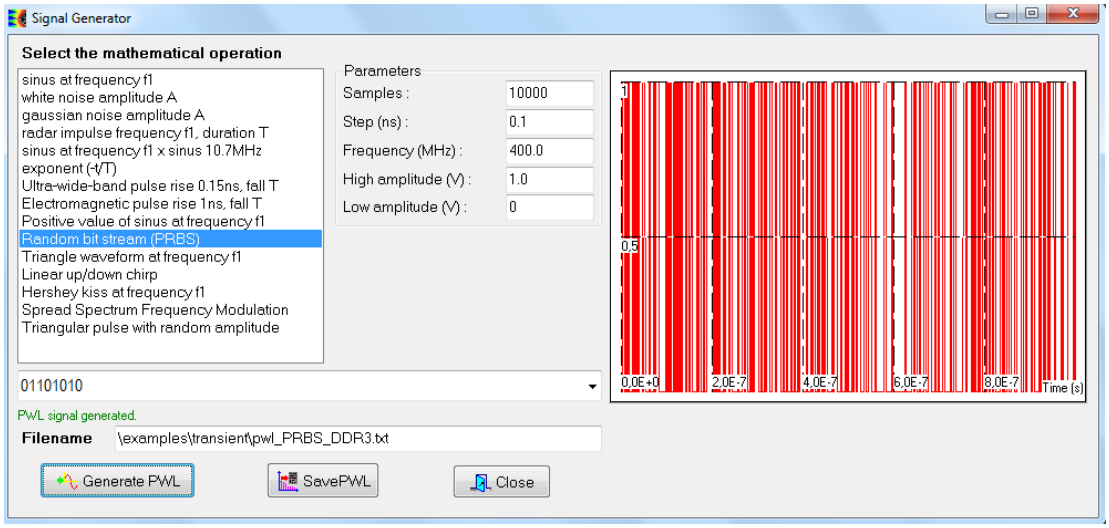


Figure 3- 48: Set a PRBS source synchronized at 400 MHz (\examples\transient\pwl_PRBS_DDR3.txt

The frequency is set to 400 MHz, i.e. the binary period is 2.5 ns. The step is 0.1 ns and 10000 samples will be generated, so that the total duration of the PWL signal will be 1 µs, corresponding to 400 transmitted bits. Click on the button "Generate PWL" to see an overview of the signal. Click on the button "Save PWL" to save the PWL file in the text file "pwl_PRBS_DDR3.txt".

On the schematic, double-click on the voltage source Vbinary to edit its properties. Select "Piece-Wise Linear" type and select the file " pwl_PRBS_DDR3.txt" in the field "Described in file". Finally, change the command line ".tran 0.1n 100 n" to ".tran 0.1n 1000n" to set a longer simulation file. The longer the simulation is, the larger the number of transmitted bits and the better the eye diagram plot.

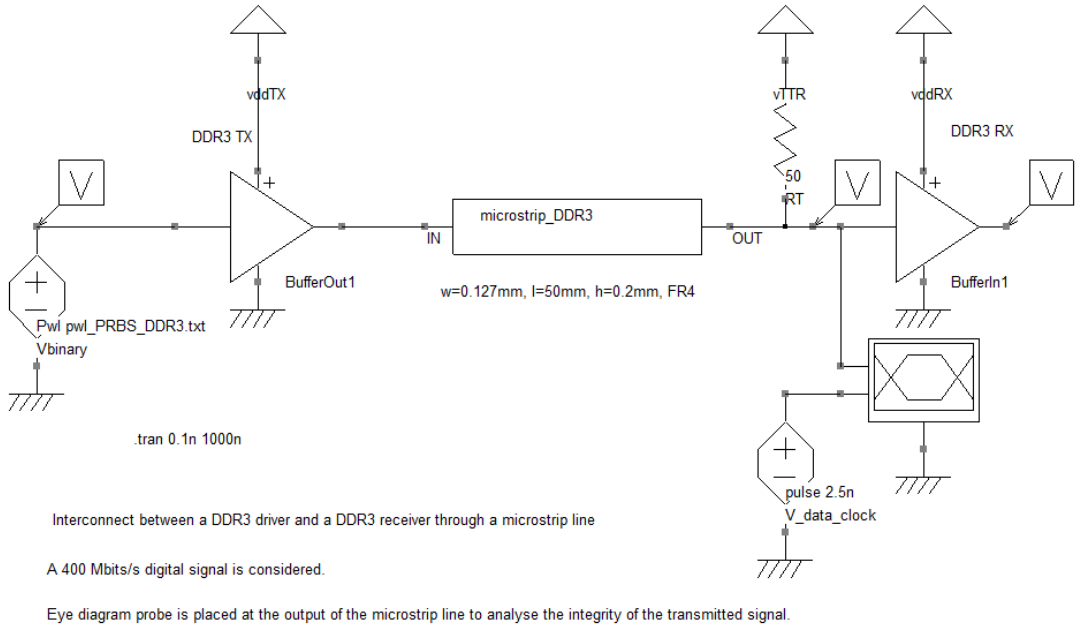


Figure 3- 49: Schematic simulation for eye diagram plotting of the DDR3 memory link (\examples\transient\ DDR3_link_400MHz_eye_diagram.sch)

III.7.5 Plot the eye diagram

In "File > Simulator", select WinSPICE and click on ▶ to generate the netlist and launch the simulation. At the end of the simulation, click on the menu "Tools > Eye Diagram" to open the eye diagram window. Select the signal to analyse in the combo box "Input signal", here v(1). The, click on the button Eye to plot the eye diagram. The result is presented in Figure 3-50. As indicated in the message bar in the bottom of the window, the input signal has been cut in 397 sections which have been superimposed to plot the eye diagram.

The field "Clock Freq (MHz)" indicates the data clock frequency extracted by the tool from transient simulation result. The value can be slightly different of the specified value in the source V_data_clock. To reduce this gap, reduce the PWL source step and transient simulation step. However, the eye diagram plot should not change significantly.

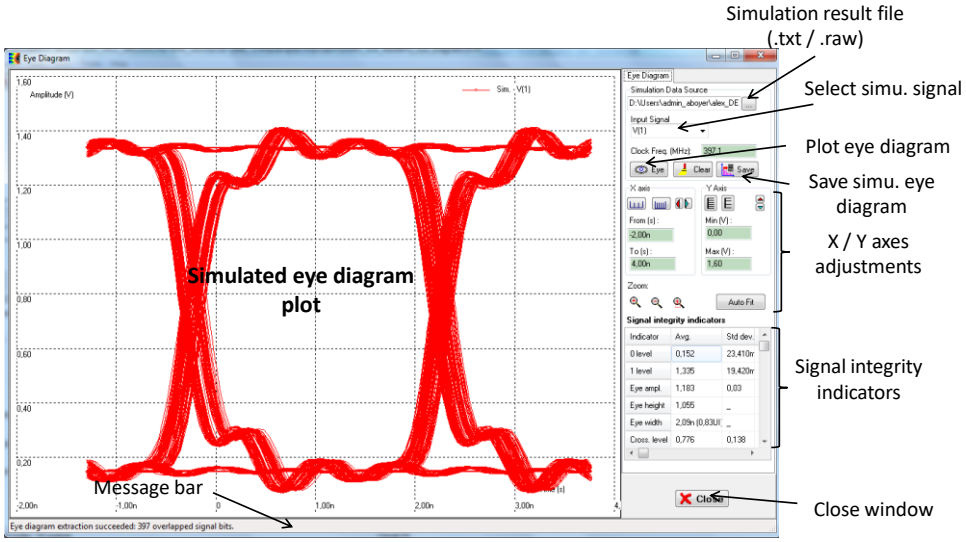


Figure 3- 50: Eye diagram of the DDR3 memory link (\examples\transient\ DDR3_link_400MHz_eye_diagram.sch)

The result shows an eye diagram with adequate horizontal and vertical apertures. However, this model does not take into account the power delivery network of both driver and receiver, which introduces non negligible inductance along the power supply network. Moreover, in a real DDR3 memory link, several data lines switch simultaneously which may introduce power significant power supply voltage drops. Moreover, crosstalk between adjacent lines could introduce additional noise. All these effects may degrade the eye diagram apertures.

In order to compare design changes on signal integrity, quantitative criteria must be defined, as those defined in III.7.1. When the eye diagram is extracted, eleven signal integrity criteria are evaluated and displayed in the table "Signal integrity indicators", in the bottom right part of the eye diagram window. For most of the criteria, average, standard deviation, minimum and maximum values are determined. For example, in this example, the vertical opening of the eye diagram (eye height) is evaluated to 1.183 V centered around nearly 0.75 V. The SNR is evaluated to 27.63. The amplitude distortion is not too large to introduce significant bit error risk. The horizontal opening of the eye (eye width) is evaluated to 2.09 ns or 0.83 UI. UI stands for 'Unit Interval', i.e. a time interval equal to the binary period. The peak-to-peak value of the jitter is about 286 ns, i.e. 11 % of the binary period.

III.8 Near-field analysis

Over the last years, the near field scanner has become a popular tool to diagnose EMC problems at PCB and IC levels. The measurement of the magnetic and electric fields near the surface of IC or PCB gives access to the current and charge surface distribution respectively, which can be helpful to understand the origin of EMC issues (conducted emission, crosstalk, radiated emission). Moreover, the measurement of the near-field emission offers a method to extrapolate the far-field emission.

In this short case study, a complex signal is generated and its characteristics are studied. An example based on a power amplifier (PA) for a 3rd generation mobile platform is used. The near-field scan measurement results are plotted with IC-EMC. Then, a near-field emission model is derived from the ICEM model of the PA. Finally, its near-field emission is simulated and compared with measurements.

III.8.1 Near-field scan measurement principles

The measurement of the electric or magnetic components in the near field is interesting for EMC of ICs because it helps to locate transient current circulation as well as strong voltage variations. Indeed, at very short distance from a conductor, it is possible to separate the respective contributions of each part of this conductor. As distance from the conductor increases, all of these contributions superimpose and only the global radiation from the conductor can be measured.

A near field scan measurement method is described in the international standard IEC 61967-3 [IEC61-3]. The typical measurement set-up with a near-field scanner is presented in Figure 3- 51. A miniature magnetic or electric antenna, called near-field probe, is placed very close to the device under test to measure the electric and/or magnetic field in the reactive or near-field area. The voltage induced across the near-field probe by the incoming field is measured by a receiver. A spectrum analyzer is usually connected to measure the amplitude of the induced voltage. The near-field probe is fixed to the arm of a 3D positioning system and its position is moved and set accurately to one measurement point, following a predefined pattern in the scan surface. For each position, the receiver captures the voltage induced across the probe (the amplitude and/or the phase of the spectrum at several frequencies, or the time domain waveform). This operation is repeated above each point of the predefined pattern. At the end of the scan surface sweeping, a near-field map is reconstructed by a post-processing tool. The map highlights some “hot spots”, i.e. areas where the incoming field is large.

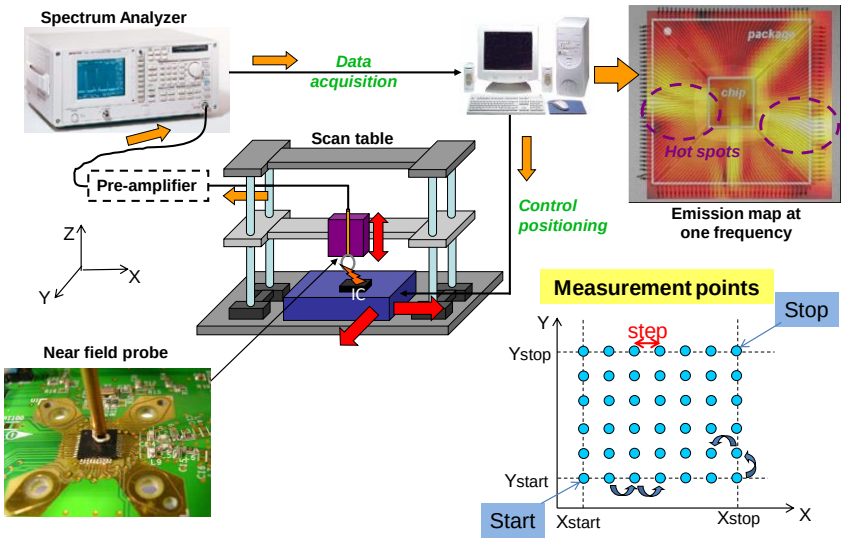


Figure 3- 51: Principle of the measurement of near-field scan emission of an IC

The near-field probes act as a transducer of electric or magnetic field into a voltage. They have various forms, but basically they consist of either small magnetic or short electric dipoles which integrate the incoming field over their surface. Ideally, the probe size should be infinitesimal in order to provide a local measurement and prevent disturbance from the incoming field. The probe should be calibrated prior near-field measurements to convert the measuring voltage into incoming electric or magnetic field.

III.8.2 Plotting near-field scan measurement with IC-EMC

The circuit studied in this part is a power amplifier (PA) used for 3rd generation or UMTS mobile platform. The PA amplifies the signals from the transceiver to the antenna. It is able to

send RF modulated signals in the frequency range 1920-1980 MHz with a maximum power of 0.25 W or 24 dBm. Three different near-field scan tests were performed above the PA with magnetic field probes to measure the horizontal Hx and Hy components and the vertical Hz component of the magnetic field. They consist in simple circular loop made at the end of a semi-rigid coaxial cable. The scan were performed at an altitude of 1.1 mm above the PA surface. The measurement area is 6.2 x 6.4 mm with X and Y steps of 0.2 mm. During these measurements, the center frequency of the UMTS power amplifier was fixed to 1950 MHz. More details about this case study can be found in [App_PA] and [Dup09].

Near-field scan measurement results were exported in a standard XML exchange file [IECTR61]. The format of this file is described in Part VI. Click on the menu "EMC > Near-field scan" or on the button  to open the "Near-field scan" interface. A window opens, with a black screen on the right for the display of measured or simulated near-field scan, and a series of tabs and buttons for simulation configurations, display options and measurement import. Click on the button 

to import a measurement file. In this example, three measurement files are provided:

- \Scan_Hx_PA_1950_1_5mm\Scan_Hx_PA_1950_1_5mm_PA.xml: measurement of the x component of the magnetic field
- \Scan_Hy_PA_1950_1_5mm\Scan_Hy_PA_1950_1_5mm_PA.xml: measurement of the y component of the magnetic field at 1950 MHz
- \Scan_Hz_PA_1950_1_8mm\Scan_Hz_PA_1950_1_8mm_PA.xml: measurement of the z component of the magnetic field at 1950 MHz

Select the file Scan_Hz_PA_1950_1_8mm_PA.xm and the results shown in Figure 3- 52 is displayed. It shows the distribution of the vertical component of the magnetic field (Hz) produced above the PA at 1950 MHz. This distribution is superimposed to a picture of the device under test. The color scale gives the amplitude of the magnetic field. The maximum magnetic field reaches up to -32 dBA/m. As indicated by the red mark. The analysis of this measurement results shows clearly that the magnetic emission is above the power output and power supply pins of the PA [Dup09]. The color scale, the zoom and the alignment of the measured scan on the background picture can be set in the tab "Display".

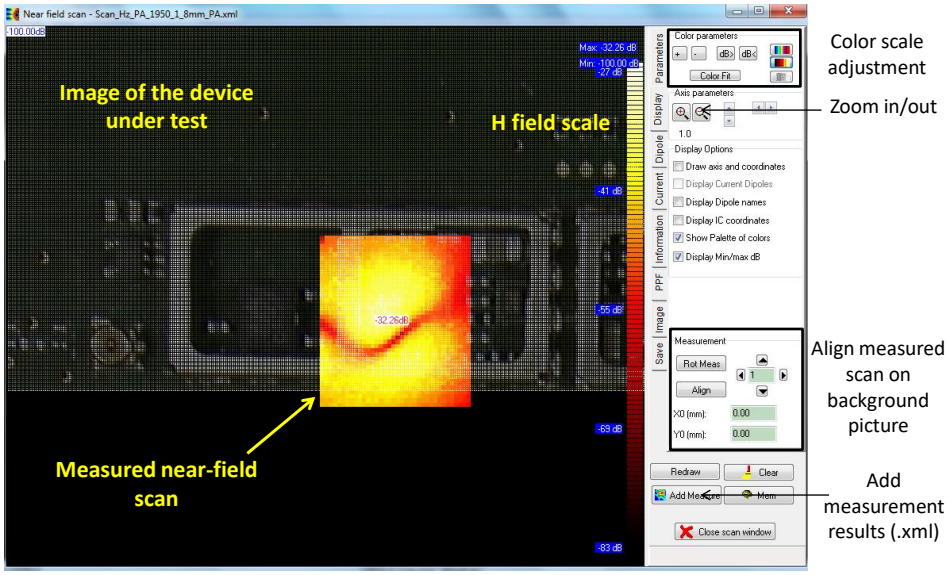


Figure 3- 52: Example of near-field scan with IC-EMC (\case_study\pa_3G\ Scan_Hx_PA_1950_1_5mm\Scan_Hz_PA_1950_1_8mm_PA.xml)

The same screen is shared for simulation result display. Once the measurement result has been imported, click on the button "Meas. scan" in the tab "Parameters" to display measurement results. The information about the imported measurement file are summarized in the tab "Information".

III.8.3 Simulating near-field emission with IC-EMC

III.8.3.1 Principle of the simulation

Various methods exist to compute EM fields produced by conductors. Three-dimensional full wave simulators are based on numerical methods that can adapt to any conductor geometry. They are the most accurate but unfortunately the most time consuming methods. In contrast, methods based on analytical formulations or geometry simplifications are very fast but they are limited only to simple geometries. The choice of an electromagnetic field solving method depends on the required accuracy level and the maximum simulation time. For example, at an early design phase, exact models cannot be available and simple calculations are often required to set some design budget. Full wave simulations can only be performed at design end for optimization purposes.

Co-simulation tools including electrical and EM simulators are required to simulate both non-linear responses and radiation of ICs. Figure 3- 53 describes the general simulation flow of this type of tool. EM fields are extracted from voltages and currents crossing metal interconnects of ICs. At IC level, package leads and bonding wires are the largest interconnects. As most of electromagnetic solvers are based on frequency domain methods, FFT algorithm is required.

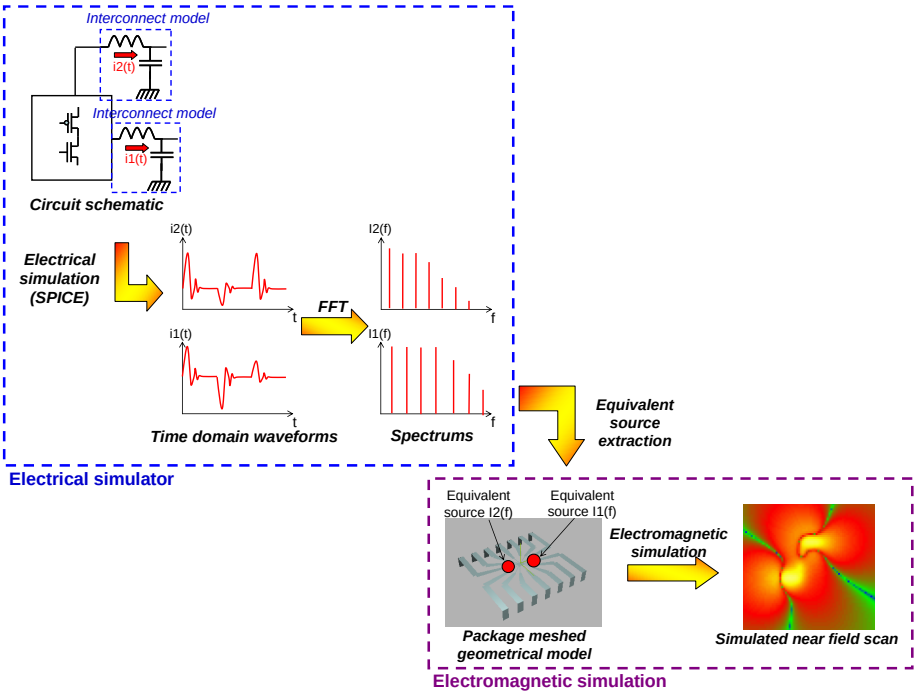


Figure 3- 53: General simulation flow for IC radiated emission prediction

IC-EMC proposes a co-simulation method to estimate near field emission from ICs. Circuit simulations are handled by WinSPICE, Ngspice or LTSPICE. An EM simulator is offered by IC-EMC to extract electrical and magnetic field at any point in (X,Y,Z) from currents and voltages computed by SPICE simulation, and by means of some approximations concerning the package and electromagnetic field formulations. The general flow used to achieve a comparison between near-field measurement and simulated magnetic field emission is proposed in Figure 3- 54. The main assumption is that package leads used for supply and output signals are the main radiating elements.

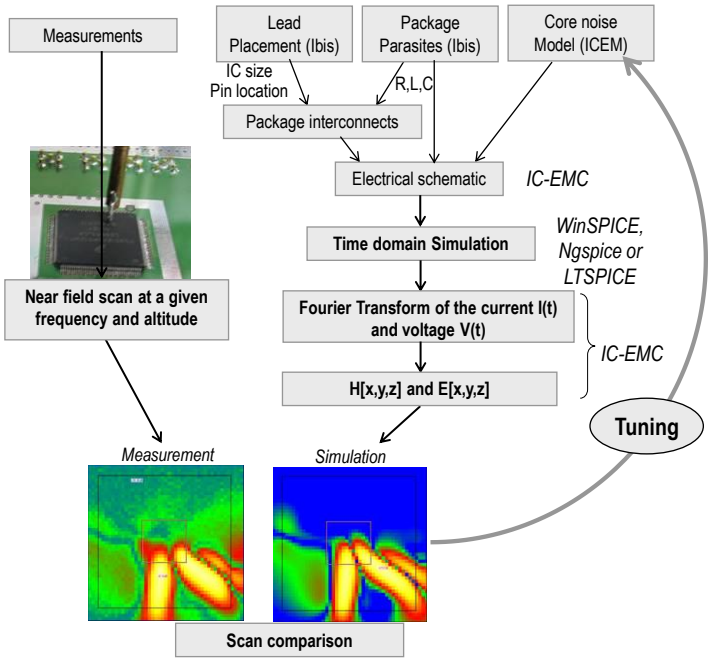


Figure 3- 54: Flow for comparing predicted and simulated magnetic field scans

At package level, leads and bonding wires are considered as the main radiated elements so that the package model is very important for the prediction of near field scan. IC-EMC uses the current computed by WinSPICE, Ngspice or LTSPICE to compute the resulting radiated emission. A link must be made between the current and the radiated elements. Two methods are used to model the radiating elements. In the first method, as the package leads and bonding wires are mainly inductive at low frequency, this link is made with the inductances which model package leads. These inductances called “radiating inductances” are classical inductances through which transient current flows, with attached geometrical coordinates. Simple geometrical models are considered for the package. Leads and bonding wires are modeled by one or several straight wires (Figure 3- 55).

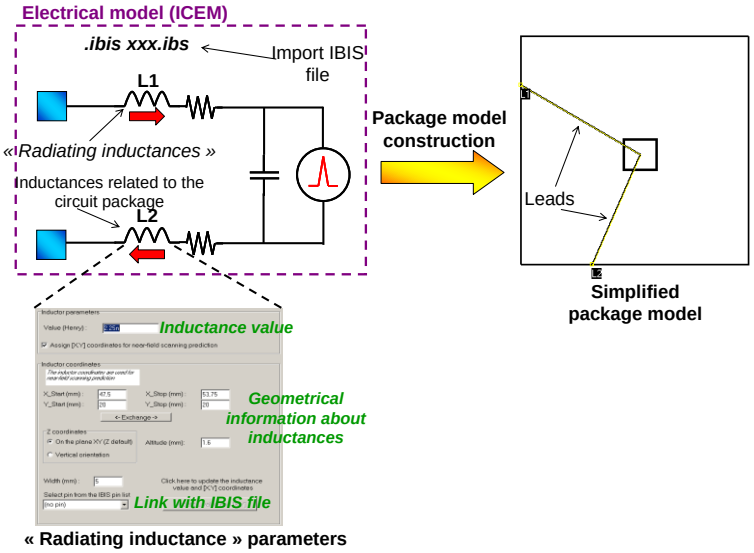


Figure 3- 55: Principles of simplified package model reconstruction and link to the electrical model through “radiating” inductances

This method assumes that the transient current circulates along electrically short interconnect, so that the “capacitive effect” of package interconnects can be neglected (i.e. charge storage). This assumption is valid until package interconnect length is less than λ/10 (quasi-static approximation). When package interconnects become electrically long, taking into account the “capacitive effect” of package interconnect become essential, especially for the prediction of electric field distribution in near-field. Indeed, a large part of electric field in near-field area is linked to charge storage, which cannot be modeled by inductance.

A more realistic electrical modeling approach consists in modeling interconnect by distributed RLC cells. IC-EMC proposes a second method for a more accurate prediction of near-field emission based on a component called “Radiated Interconnect”, available in the Symbol Palette  . They are not described here. More information can be found in [App_NF].

The geometrical information of “radiating inductances” can be entered manually or given by IBIS file (see part III.5). The package and die size information text are added in the [package model] section of the IBIS file. The comment is mandatory to avoid parsing errors with conventional IBIS readers. However, IC-EMC can locate ‘|pack_’ and ‘|ic_’ keywords and get the relevant information. The 2D and 3D views of the package may then be reconstructed, as shown in Figure 3- 35.

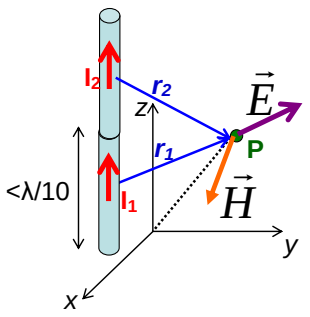
III.8.3.2 Near-field Prediction Steps

Assuming that the package bonding wires and leads are the main radiating elements, their associated current must be computed, prior to magnetic field reconstruction (and also charge storage for electric field reconstruction). Therefore, the simulation steps are as follows:

1. The IBIS file is loaded, from which the pin list, package dimension and type are extracted
2. From the IBIS information, the package is reconstructed. Each lead is assigned a position in space.
3. Selected inductances (mainly supply and IO inductances) are assigned to the corresponding space coordinates (or select radiated interconnects).
4. The analog time-domain simulation is performed to determine all the currents flowing in each declared package inductances.
5. The Fourier transform applied for each of these currents gives the magnitude I(f) for a frequency chosen for scanning.
6. Theoretical formulations are used to compute the sum of H and E contributions at each location of the space [x,y,z] in frequency domain.
7. A post-processing displays the resulting magnetic field at the user-defined distance above the ground plane.

III.8.3.3 Formulations used to compute near-field emission

Formulations used by IC-EMC to compute electric and magnetic fields radiated by a package are based on the thin wire approximation. They are computed in frequency domain. Each lead of a package is meshed in small elementary thin wire crossed by a current constant over all the lead. This assumption remain valid until the lead length is negligible in comparison to the wavelength λ (length < λ/10). The electric and magnetic fields generated by of each elementary wire are calculated from the equations reported in Figure 3- 56. Parameters are the length of the current element *l*, the current amplitude *I0* in the element (A), and $\omega=2\pi.f$ (rad/s). The magnetic current at the observation point is the sum (in complex domain) of all elementary currents flowing in all leads.



$$\vec{A}=\frac{\mu}{4\pi}\times\int_{-L/2}^{L/2} I(z)\frac{e^{-j\beta r}}{r}dz\,\vec{z}$$

$$\Phi=\frac{1}{4\pi\varepsilon_0\varepsilon_r}\times\int_{-L/2}^{L/2} Q(z)\frac{e^{-j\beta r}}{r}dz$$

$$\vec{H}=\frac{1}{\mu}\nabla\times\vec{A}$$

$$\vec{E}=-j\omega\vec{A}-\vec{\nabla}\Phi$$

Figure 3- 56: Electric and magnetic field formulations with the thin wire approximation

If the package lead is longer than λ/10, the package is split into elementary dipoles as shown in Figure 3- 57. The electric and magnetic current at the observation point are the sum (in complex domain) of all elementary currents flowing in the package leads.

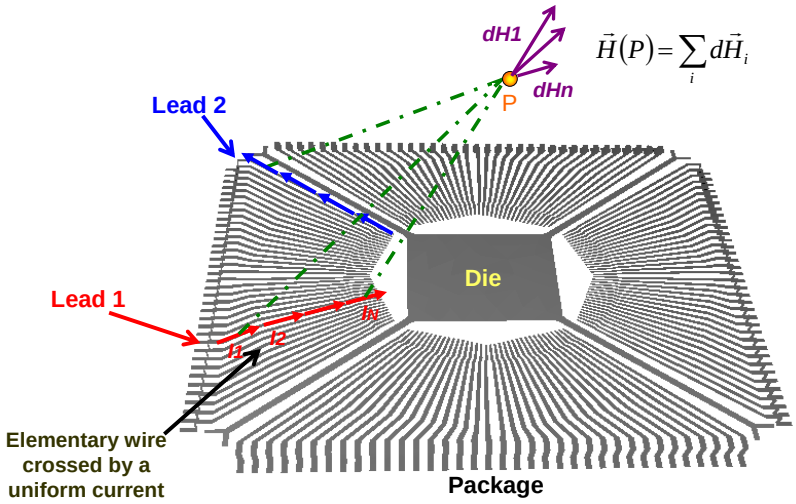


Figure 3- 57: Decomposition of package leads in elementary thin wires and contribution to the total electric and magnetic fields

III.8.4 Near-Field Prediction

In this part, the different steps to load the model, run the simulation and compute the near-field emission are presented.

III.8.4.1 Load the simulation model

The model of the PA for its near-field simulation is given in the file " \case_study\pa_3g\ PA_scan_V_add_vertical_1950MHz.sch". The electrical schematic diagram is presented in Figure 3- 58. It includes the supply network, the PDN of the PA, the pre-amplifier stage and the power stage itself, connected to a 50 Ω through a transmission line. Note that the PA itself is mainly a current source.

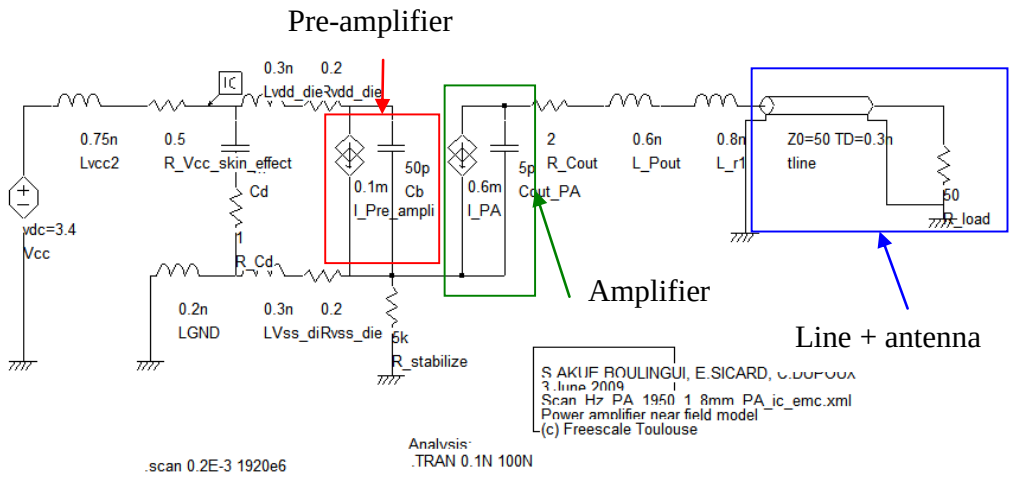


Figure 3- 58: The schematic diagram of Prometheus used for near-field scan prediction (case_study\pa_3G\PA_scan_V_8_1950MHz.sch)

The position of the package leads are deduced from the IBIS file. Normally, the IBIS file of the PA is imported automatically when the schematic is opened thanks to the command line ".ibs .ibis prometheus_mmm6030_v2.ibs". If a warning message indicates that the IBIS file is

not found, you can import it manually with the command "File > Load Ibis file" or with the button [Ibs] in the command bar. Figure 3- 59 shows a 3D reconstruction of the PA package visible in the IBIS interface (see part III.5.3.3). The position of the different pins can be highlighted.

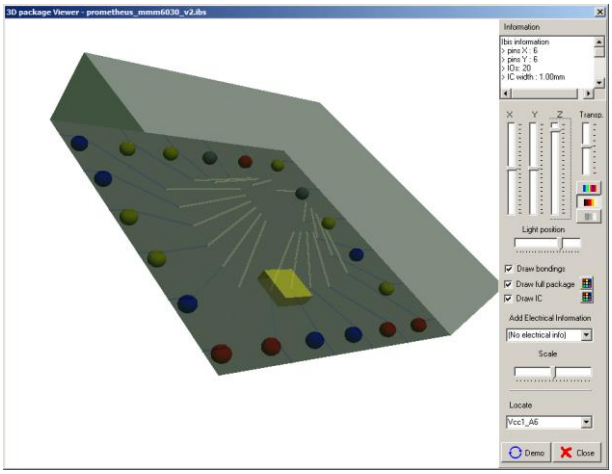


Figure 3- 59: 3D view of the PA package (\case_study\pa_3G\ prometheus_mmm6030_v2.ibs)

Figure 3- 60 details how the package lead inductances are assigned physical coordinates to enable the IC-EMC simulator to compute the radiated field. You can define it manually by typing the coordinates in the "Xstart", "Ystart", "Xstop", "Ystop", "Zstart" and "Zstop", or using IBIS information by selecting a pin in the list "Select pin from the IBIS pin list". The Z coordinate indicates the altitude of the dipoles above a plane reference which is supposed to be the surface of the PCB on which the circuit is mounted.

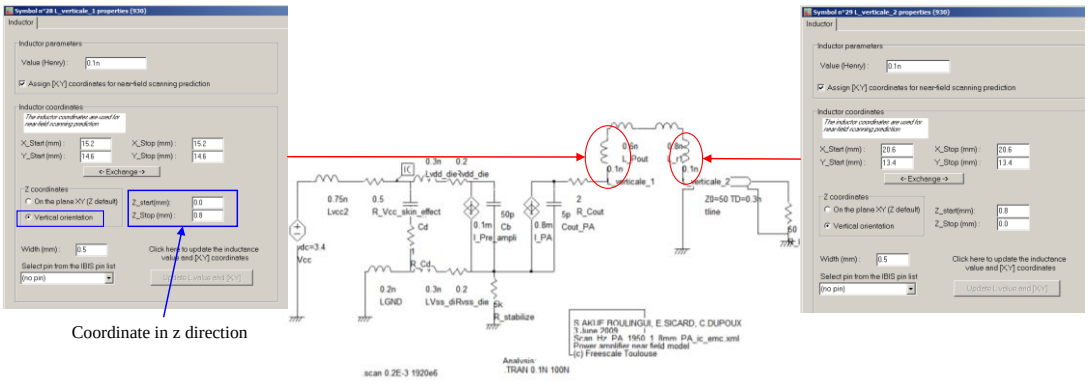


Figure 3- 60: The schematic diagram of Prometheus used for near-field scan prediction (Scan_Hx_PA_1950_1_5mm\PA_scan_V_add_vertical_1950MHz.sch)

III.8.4.2 Preparing SPICE simulation

The near-field simulation is based on the transient waveform of currents and voltages across radiated interconnects. A transient simulation is configured with the command line " .TRAN 0.1N 100N". It can be inserted according one of the two following methods:

- click on button **A** or in the "Edit > Text" menu, directly type the SPICE analysis command
- in the Insert menu, click on “Insert analysis line”. An interface dedicated to the configuration of the SPICE simulation is opened and the analysis line is automatically inserted on the schematic with the correct syntax.

Another command line is inserted on the schematic: " . scan 0.5e-3 1e8 2e8 2 3.5e-3 1.2e-3". It contains directive for the near-field simulation tool. The parameters of the command line will be described in part III.8.4.4.

III.8.4.3 Run SPICE simulation

Select WinSPICE as simulator in "File > Simulator". In the menu "File > Simulator > Configurations", select "Interactive mode" to launch SPICE simulation automatically after the SPICE netlist generation  .

III.8.4.4 Near-field simulation

Open the "Near-field scan" interface by clicking on the button  or in the menu "EMC > Near field scan". The window shown in Figure 3- 61 opens. In the right part, the simulation parameters and the display options can be configured. In the left part, the position of the radiatng dipoles or interconnects and the simulated or measured E or H field are plotted in a X-Y surface at a given altitude. Different components of the fields can be plotted (x, y, z, tangential, total), either the amplitude (in dBV/m or dBA/m) or the phase (in degree). When the window is opened, no simulation or measurement results have been loaded, so the screen is black.

The default opened tab is "Parameters" for the configuration of the simulation and the selection of frequency and field component to display. Clicking on the button "Far field" computes the far-field emission in two vertical planes. The tab "Display" is dedicated for the control of measurement or simulation result plot (zoom, scale color, scale adjustement...). In the tab Dipole, the amplitudes of the excitation currents of the radiating dipoles at the simulation frequency are listed. In the tab "Save", several options to save simulated scans in a XML file are proposed. 2D graph of the near-field emission can be displayed if the button "2D graph" is clicked.

The simulation options in the tab "Parameters" are preconfigured because of the command line ".scan 0.5e-3 1e8 2e8 2 3.5e-3 1.2e-3" placed in the schematic diagram. The format of this command line is:

```
.scan step start_freq stop_freq freq_nb scan_alt dipole_alt
```

where:

- step is the scan step. In this example, the field is computed with a spatial resolution of 0.5 mm.
- start_freq, stop_freq and freq_nb define the frequency sweep between start_freq and stop_freq. freq_nb defines the number of frequency points of the simulation
- scan_alt defines the altitude of the scan plane, i.e. the distance above the reference plane where the field values are computed
- dipole_alt is the default altitude of the radiated dipoles and interconnects if it is not defined.

We remind here that the reference plane is the surface of the PCB on which the circuit is mounted. Depending on the selection of the option "Ground plane at z = 0", a perfect ground plane can fill the reference plane.

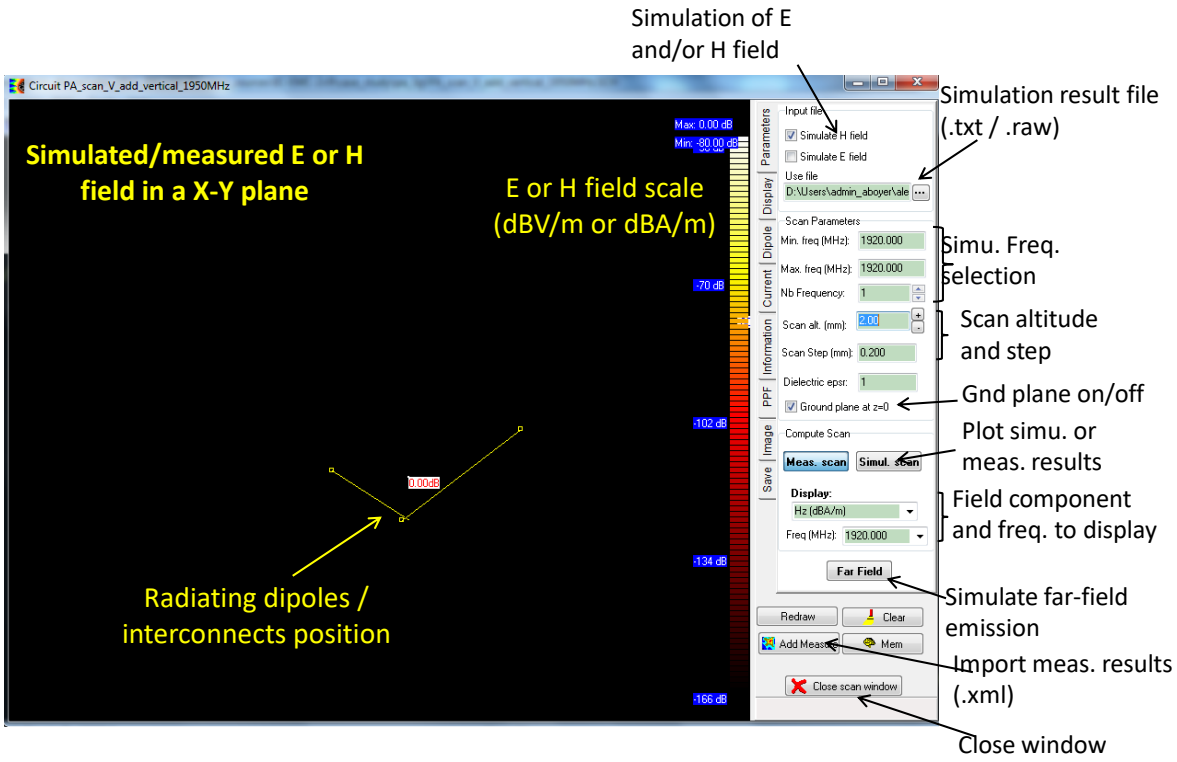


Figure 3- 61: Near-field scan interface (Scan_Hx_PA_1950_1_5mm\PA_scan_V_add_vertical_1950MHz.sch)

Before launching the computation, verify the parameters of the simulation: frequencies, scan altitude, ground plane, scan step, position of dipoles. Click on the button Simul. scan to launch the computation. It can take several minutes depending on the number of dipoles and frequency points.

At the end of the computation, the total magnetic field (Htot in the combo box "Display") at F = 1920 MHz is plotted. In the tab "Display, the scale and the position of the scan are can be adjusted. Figure 3- 62 presents the vertical component of the magnetic field Hz simulated at 1920 MHz.

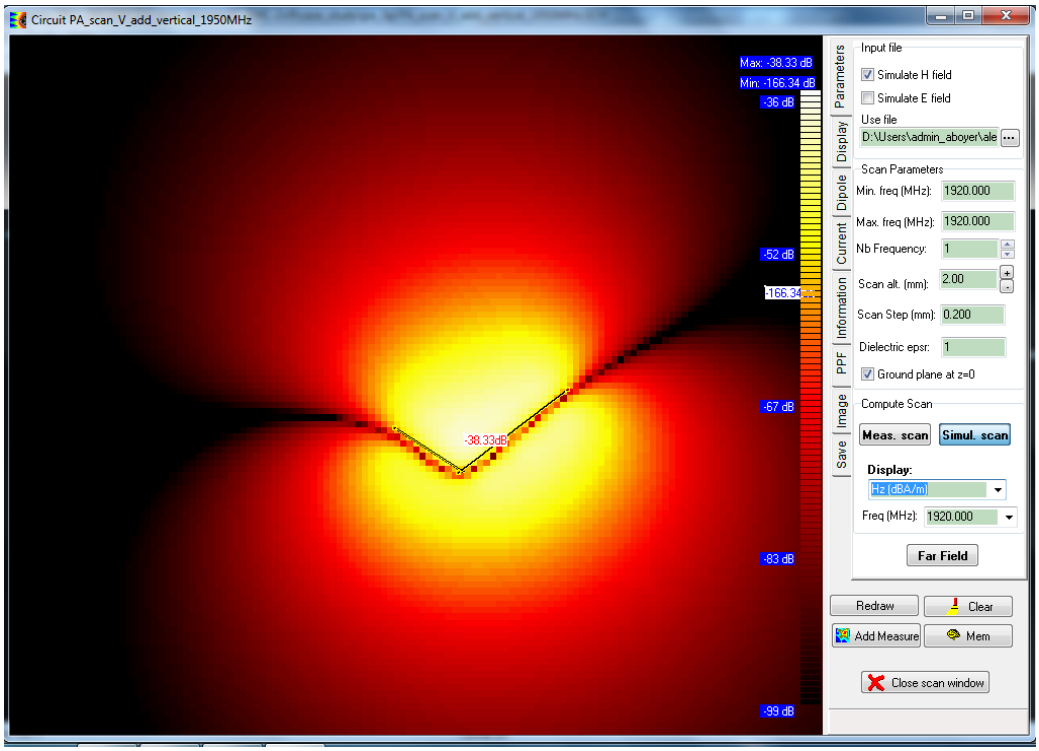


Figure 3- 62: Simulation of the vertical components of the magnetic field Hz simulated at 1920 MHz (Scan_Hx_PA_1950_1_5mm\PA_scan_V_add_vertical_1950MHz.sch)

A comparison between measurements and simulations is presented in Figure 3- 63. The differences are summarized in Table 3- 9.

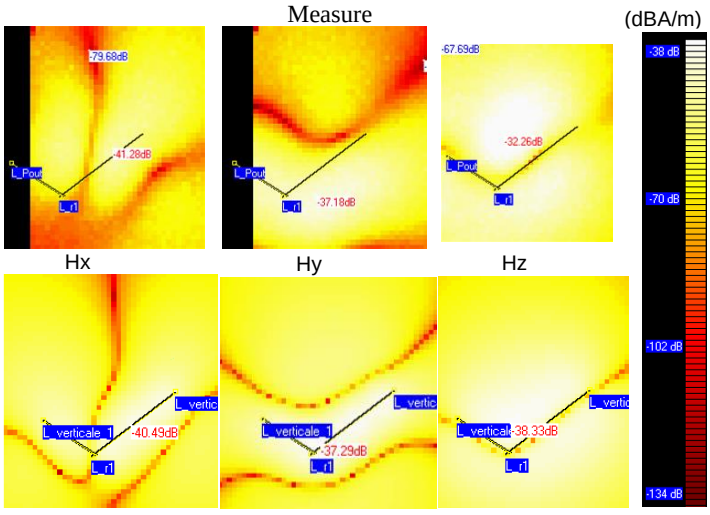


Figure 3- 63: Comparison between measurements and simulations of the three components of the magnetic field (Scan_Hx_PA_1950_1_5mm\PA_scan_V_add_vertical_1950MHz.sch)

Measurement	**Hx**	**Hy**	**Hz**
	-41 dBA/m	-37 dBA/m	-32 dBA/m
Simulation	**Hx**	**Hy**	**Hz**

	-40 dBA/m	-37 dBA/m	-38 dBA/m

Table 3- 9: Comparison between measured and simulated peak magnetic field

III.9 Interconnect modeling

Modeling Interconnect at package, PCB or system level is a very important task to predict EMC issues. IC-EMC proposes several tools to evaluate stray R, L, C parameters and build equivalent electrical models of basic types of electronic interconnects, at different levels:

- PCB traces and planes
- package
- cables

The following sections presents these tools through simple examples.

III.9.1 Modeling a microstrip line designed on a FR4 PCB

In this part, a SPICE compatible model of a microstrip line will be constructed in order to simulate S parameters from its terminals. The geometry and the parameters of the line are described in Figure 3- 64. The final model is available in the file "\examples\basic\microstrip_S_parameters.sch". The following parts will guide you to build the model step-by-step.

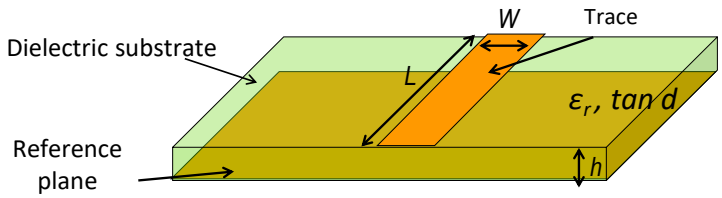


Figure 3- 64: Geometry of the modeled microstrip line

The microstrip line is designed on a 0.2 mm thick FR4 substrate. The relative permittivity of the substrate is ε_r = 4.5 and its loss tangent tan d = 0.02. The trace is made of 35 µm thick copper. The trace is 50 mm long and its width must be adjusted to match its characteristic impedance Z_0 to 50 Ω. The model must be valid up to 20 GHz.

III.9.1.1 Open the tool "Interconnect Parameters"

The tool "Interconnect Parameters" is dedicated to the modeling of PCB interconnects with basic cross-section (e.g. microstrip line, coplanar waveguide, edge-coupled microstrip line, via…) and the construction of equivalent electrical model. Click on the menu "Tools > Interconnect Parameters" to launch this tool. The following window appears, with microstrip line as default configuration.

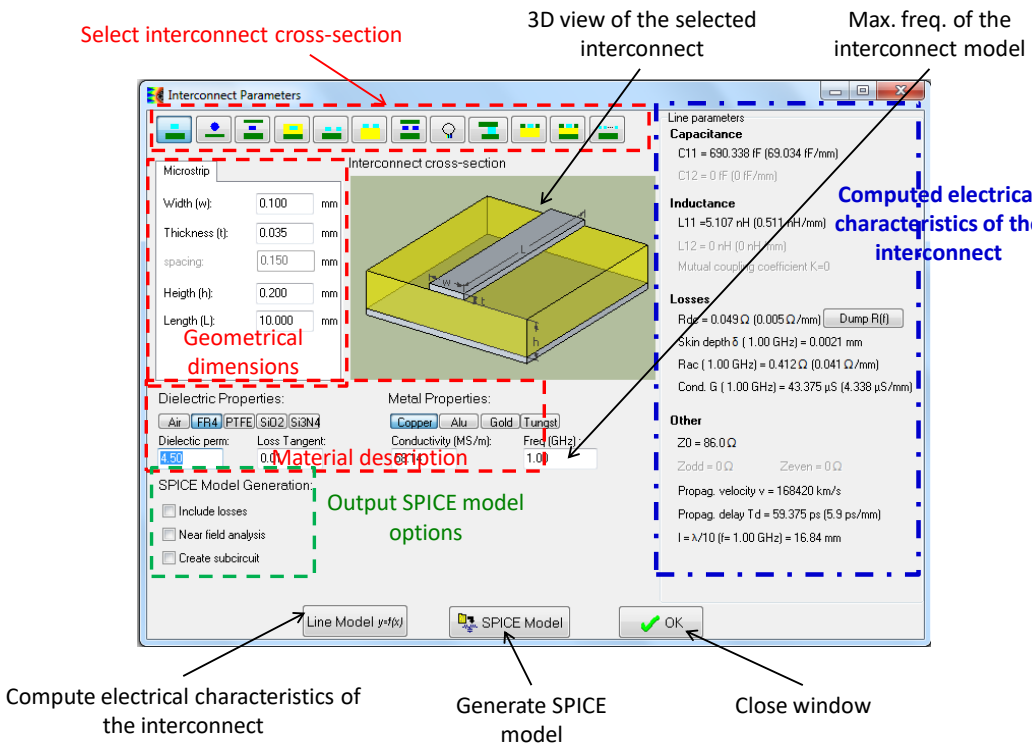


Figure 3- 65: Description of "Tools > Interconnect Parameters"

In this tool, the cross-section and the material are supposed to be homogeneous. Modeling an interconnect requires the definition of cross-section geometry, the interconnect length, the material electrical properties (trace metal and dielectric insulator) and a maximum validity frequency (some parameters are frequency dependent). Once these parameters have been defined, the electrical characteristics of the interconnect can be extracted from closed-form expressions or numerical computations, such as:

- per-unit-length (pul) electrical parameters r, l, c and g
- characteristic impedance, odd and even impedance (for three conductor interconnects)
- wave velocity and propagation delay
- skin depth

Finally, SPICE compatible models can be derived from these computed elements.

III.9.1.2 Electrical parameter extraction

The microstrip line must be 50 Ω matched. In practical PCB design, the trace's width W is adjusted to set the characteristic impedance. In Interconnect Parameters, fill the geometrical dimensions and the material properties according to the description given in III.9.1. Start with a default value for the width, equal to 0.1 mm. Then, click on the button Line Model y=f(x) to compute the electrical characteristics of the line, which appear on the right side of the screen. In this default configuration, the characteristic impedance is given by the term "Z0" and is equal to 86 Ω.

Increase the width to reduce the characteristic impedance. It should be equal to 50 Ω when the width is set to 0.347 mm, as shown in Figure 3- 66.

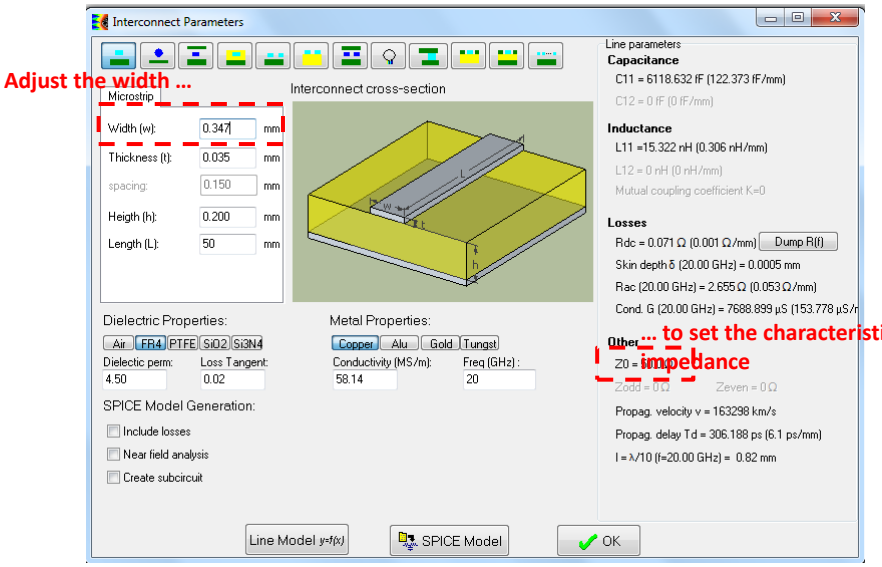


Figure 3- 66: Adjustment of the trace's width to set the characteristic impedance of the microstrip line

The pul r,l,c,g parameters of the line are also computed. The pul inductance and inductance of the lines are given by the terms "L11" and "C11". We can verify that the characteristic impedance is equal to:

$$Z_0 = \sqrt{\frac{L_{11}}{C_{11}}} \qquad \textit{Equ. III-8}$$

The pul resistance and conductance are actually frequency dependent (even if L11 is also slightly frequency dependent due to skin effect). The term "Rdc" gives the pul resistance at low frequency, when the skin effect is negligible i.e. when the lateral dimensions of the line are smaller than the skin depth δ. For example, at 20 GHz, the skin depth is 0.5 µm so that this effect cannot be neglected. The pul resistance tends to increase with frequency according to a square-root relation. The term "Rac" gives the actual pul resistance at the maximum validity frequency of the model (here 20 GHz). The frequency evolution of the skin depth and Rac can be saved in a .z file by clicking on the button Dump R(f).

Similarly, the term "G" gives the conductance associated to dielectric substrate losses at the maximum validity frequency of the model.

III.9.1.3 Extraction of a SPICE compatible model

From the pul parameters, a SPICE compatible model can be derived. A short section of a transmission line can be modeled by a lumped RLCG model. The model remains valid as long as the length of the section is less than λ/20 or λ/10, where λ is the wavelength associated with the highest frequency of the signal conducted along the line. Thus, the full model of the line consists of a distribution of this RLCG network.

In Figure 3- 66, the last line of the right part of the screen l = λ/10 (f=20.00 GHz) = 0.82 mm gives the maximum length of a line section which can be modeled by a single RLCG network up to 20 GHz. As the microstrip line is 50 mm long, 50/0.82 = 61 RLCG networks are required to model the microstrip line up to 20 GHz.

Before generating the SPICE model, several options may be chosen. They are visible on the lower left part of the this screen ("SPICE Model Generation"):

- Include losses: if the option is not selected, only the DC resistance of the line is taken into account, the skin effect and dielectric losses are neglected. This assumption is usually valid with practical PCB traces up to several hundreds of MHz. Above several GHz, losses should be taken into account, especially for signal integrity simulation
- Near-field analysis: if this option is selected, geometrical coordinates are assigned to each RLCG network of the model in order to simulate the electric and magnetic field emission produced by currents circulating along the line (refer to III.8).
- Create subcircuit: if this option is selected, the SPICE model is saved in a subcircuit. Otherwise, RLCG networks are placed directly on the schematic.

For the studied microstrip line, check "Include losses" to include frequency dependent losses in the model, and leave "Near-field analysis" unchecked. Initially, we let the option "Create subcricuit" unchecked. Click on the button SPICE Model to generate automatically the equivalent model of the line. Then click on the button OK to close the window. A large number of RLCG networks have been placed on the schematic, as shown in . Click on the button all to see all the RLCG networks. 62 RLCG networks have been placed.

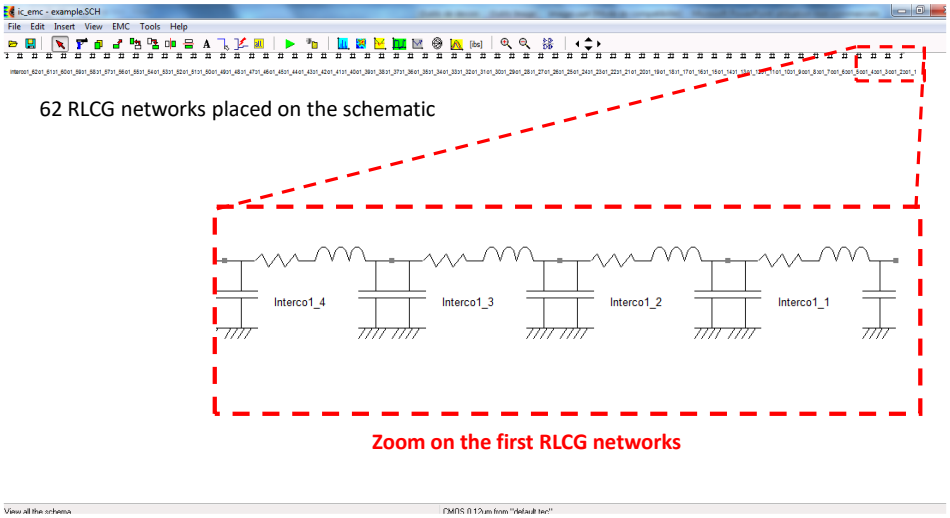


Figure 3- 67: Electrical model of the microstrip line valid up to 20 GHz

The advantage of this model display is that the content of the model is visible explicitly. However, at high frequency, the number of RLCG cells may become large sufficiently to make it unreadable. Therefore, it is better to select the option ""Create subcircuit".

Remove all the RLCG networks placed on the schematic with the symbol . Then open the "Interconnect Parameters" tool and fill all the fields as in Figure 3- 66. Check the option "Create subcircuit". A field "Save subcircuit as:" appears to specify the name of the subcircuit file. Click on the button ... to select the directory and the file name. The subcircuit is saved in .sym file. The microstrip line model has been saved in "\example\basic\microstrip_20GHz.sym". Finally, click on the button SPICE Model to save the SPICE model in the .sym file. This time, no model is placed automatically on the schematic. Click on OK to close the window.

III.9.1.4 S parameter simulation

Click on the menu "Insert > User symbol (.SYM)" to place the subcircuit of the microstrip line on the schematic. Select the file "\example\basic\microstrip_20GHz.sym". A rectangular box with three terminals with the title "microstrip_20GHz" is placed on the schematic: the terminals "io1" and "io2" are the two terminals of the trace, while "io_ref" is the ground plane. If you double-click on the symbol, the SPICE subcircuit can be edited (only in readable mode).

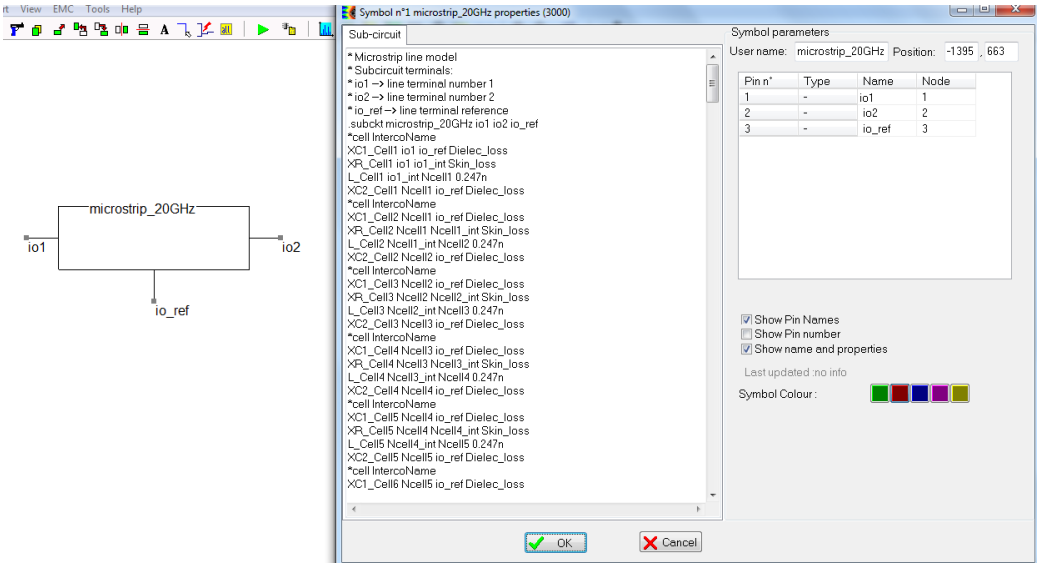


Figure 3- 68: Microstrip line subcircuit (\Examples\basic\PCB\microstrip_20GHz.sym)

To do a S parameter simulation, connect "io_ref" to the ground and connect two S parameter probes on trace terminals as described in part III.3. Set an .AC simulation with the SPICE analysis command ".AC DEC 50 1MEG 20G". The schematic is shown in Figure 3- 69.

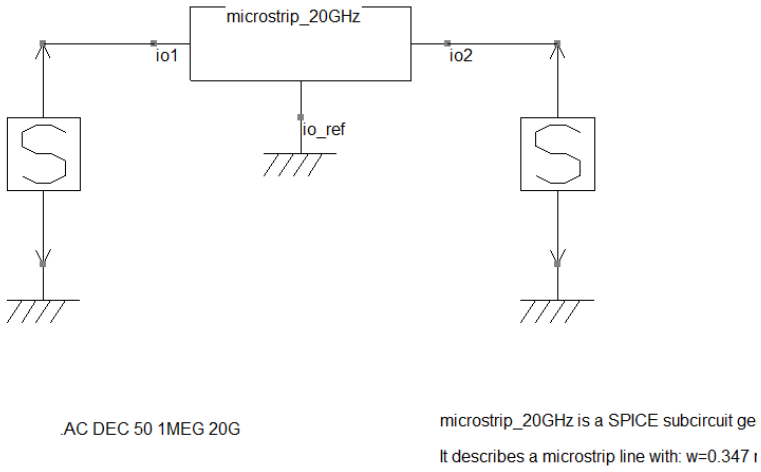


Figure 3- 69: S parameter simulation of microstrip line (\Examples\basic\PCB\microstrip_S_parameters.sch)

Select WinSPICE as simulator and click on the button  to launch the simulation. At the end of the simulation, click on the button  to open the S parameter window. Plot the S11 and S12 parameters, as shown in Figure 3- 70. In spite of the 50 Ω matching of the line, the reflection coefficient S11 is not null and tends to increase with frequency, because of the frequency dependent loss of the line. Similarly, the transmission coefficient is nearly equal to

1 up to several hundreds of MHz, but tends to decrease with frequency due to losses. The multiple minima visible on the S11 curve are due to the line resonances.

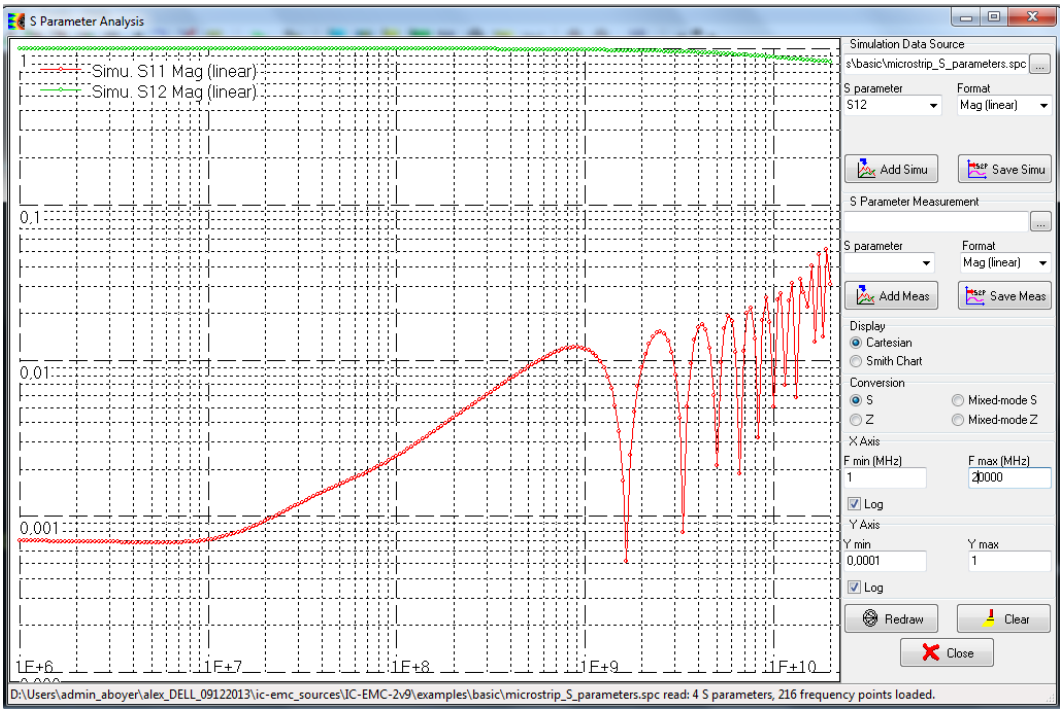


Figure 3- 70: S parameter simulation of microstrip line (\Examples\basic\PCB\microstrip_S_parameters.sch)

III.9.2 Cable modeling

This tool is similar to "Interconnect Parameters", except it is dedicated to cable modeling. The tool builds electrical model of cables with basic cross-section (e.g. coaxial cable, bifilar cable, shielded pair…). Click on the menu "Tools > Cable Modeling" to launch this tool. The following window appears, with microstrip line as default configuration. In this tool, the cross-section and the material are supposed to be homogeneous. Modeling an interconnect requires the definition of cross-section geometry, the cable length, the material electrical properties (trace metal and dielectric insulator) and a maximum validity frequency (some parameters are frequency dependent). Once these parameters have been defined, the electrical characteristics of the cable can be extracted from closed-form expressions or numerical computations, such as:

- per-unit-length (pul) electrical parameters r, l, c and g
- characteristic impedance, odd and even impedance (for three conductor interconnects)
- wave velocity and propagation delay
- skin depth

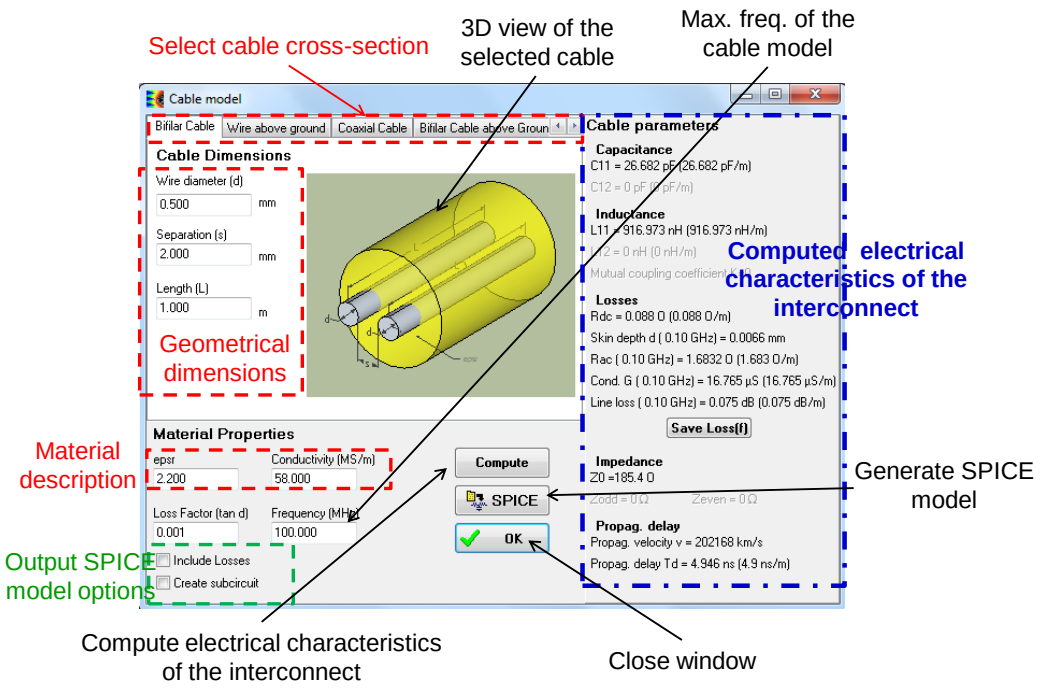


Figure 3- 71: Description of "Tools > Cable Modeling"

Finally, SPICE compatible models can be derived from these computed elements. As with "Interconnect Parameters", the generated SPICE model can be exported in a subcircuit.

In the following part, we consider the case study described in Figure 3- 72. It consists in a bibfilar pair placed at a distance h above a ground plane. The final model is available in the file "\examples\basic\bif_above_gnd_1m.sch". The following parts will guide you to build the model step-by-step.

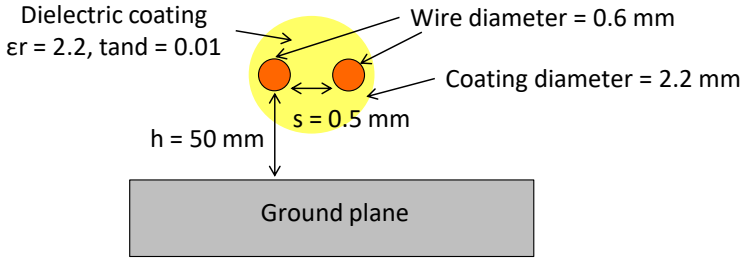


Figure 3- 72: Geometry of the modeled cable

The cable is composed of two 0.6 mm large wires embedded within insulator coating. The coating has a relative permittivity of the substrate equal to $\varepsilon_r = 2.2$ and a loss tangent tan d = 0.01. The cable is 1 m long. The model must be valid up to 300 MHz.

III.9.2.1 Electrical parameter extraction

In "Cable Modeling", select the cross-section "Bifilar Cable above Ground Plane" and fill the geometrical dimensions and the material properties according to the description given in III.9.2. Then, click on the button **Compute** to compute the electrical characteristics of the line, which appear on the right side of the screen, as shown in Geometry of the modeled cableFigure 3- 72. Three terms related to characteristic impedance appear:

- Zodd: odd-mode impedance
- Zeven: even-mode impedance
- Z0: characteristic impedance in single-mode excitation

The differences between these impedance terms can be understood when the propagation analysis along the cable is made. Both wires and the reference plane actually form a three-conductor transmission line. The wires can be excited according to three different modes:

- single-ended mode: one wire is excited while the other is set to 0 V (the reference plane potential)
- differential mode: both wires are driven with equal but opposite voltages
- common mode: both wires are driven with the same voltage

A convenient method for analysing the propagation through the line is to decompose the propagation modes into two virtual propagation modes: the odd and even modes. Whatever the line excitation, the actual current and voltage distribution along this line can be expressed as a superposition of odd and even modes. Both are characterized by characteristic impedances (Zodd and Zeven) that may be expressed according to the per unit length parameters r, l, c, g of the line. Differential, common-mode and singled-ended characteristic impedance are related to Zodd and Zeven according to equations III-8 to III-10.

$$Z_{Diff} = 2.Z_{odd} \quad \textit{Equ. III-9} \qquad Z_{comm} = \frac{1}{2} Z_{even} \quad \textit{Equ. III-10} \qquad Z_0 \approx \sqrt{Z_{odd} Z_{even}} \quad \textit{Equ. III-11}$$

As signals are usually transferred differentially, the differential-mode impedance and thus odd-mode impedance must be known and controlled properly to ensure a correct impedance matching. With the dimensions, the odd-mode impedance is nearly 60 Ω, so that the differential-mode impedance of the cable is 120 Ω. A 120 Ω termination should be placed to avoid any reflections.

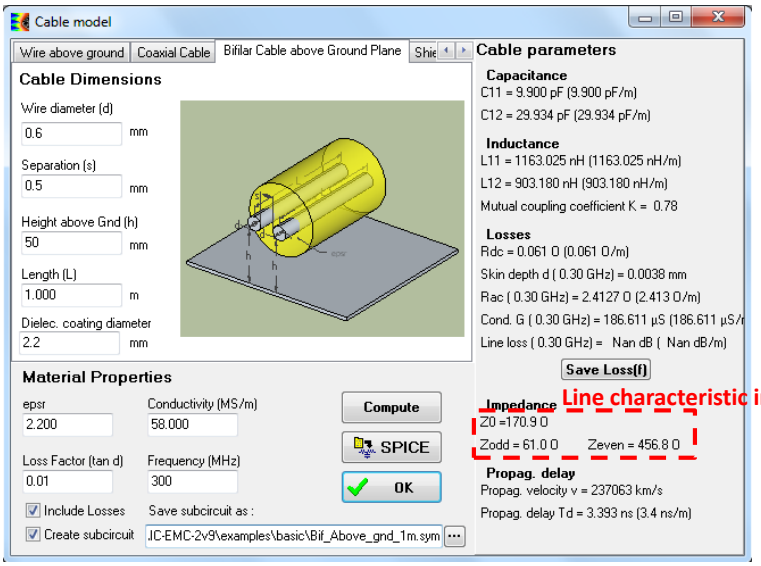


Figure 3- 73: Extraction of the electrical characteristics of the cable

The pul r,l,c,g parameters of the line are also computed. As in "Interconnect Parameters", the pul resistance and conductance are actually frequency dependent. They take into account skin effect and dielectric losses.

III.9.2.2 Extraction of a SPICE compatible model

From the pul parameters, a SPICE compatible model can be derived. Similarly to PCB interconnect models built with "Interconnect Parameters", it is based on distributed RLCG networks, where each RLCG network models an electrically short section of cable.

Before generating the SPICE model, two options may be chosen. They are visible on the lower left part of the this screen ("SPICE Model Generation"):

- Include losses: if the option is not selected, only the DC resistance of the wires is taken into account, the skin effect and dielectric losses are neglected. This assumption is usually valid with practical PCB traces up to several hundreds of MHz. Above several GHz, losses should be taken into account, especially for signal integrity simulation
- Create subcircuit: if this option is selected, the SPICE model is saved in a subcircuit. Otherwise, RLCG networks are placed directly on the schematic.

Select both options. Specify the name of the subcircuit in the field "Save subcircuit as:". Click on the button ... to select the directory and the file name. The subcircuit is saved in .sym file. The microstrip line model has been saved in "\example\basic\ \Bif_Above_gnd_1m.sym.sym". Finally, click on the button SPICE Model to save the SPICE model in the .sym file. Click on OK to close the window.

III.9.2.3 S parameter simulation

Click on the menu "Insert > User symbol (.SYM)" to place the subcircuit of the microstrip line on the schematic. Select the file "\example\basic\Bif_Above_gnd_1m.sym". A rectangular box with five terminals with the title "Bif_Above_gnd_1m" is placed on the schematic: the terminals "io1_1" and "io1_2" are the two terminals of one wire, "io2_1" and "io2_2" are the two terminals of one wire, while "io_ref" is the ground plane. If you double-click on the symbol, the SPICE subcircuit can be edited (only in readable mode).

To do a S parameter simulation, connect "io_ref" to the ground and connect four S parameter probes on cable terminals as described in part III.3. Set an .AC simulation with the SPICE analysis command ".AC DEC 50 100k 300MEG". The schematic is shown in Figure 3- 74.

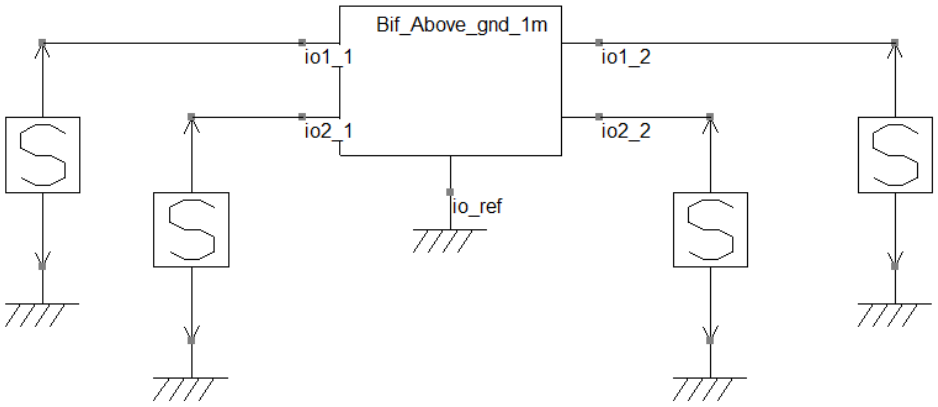
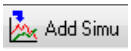


Figure 3- 74: S parameter simulation of a bifilar pair cable (\Examples\basic\Cables\Bif_above_gnd_1m.sch)

Select WinSPICE as simulator and click on the button to launch the simulation. At the end of the simulation, click on the button to open the S parameter window. Single-ended S parameters are plotted by default. However, it can be interested for a transmission line with

more than two conductor to plot mixed-mode S parameters. Instead of considering the reflection or transmission coefficients at or between each line terminal according to the reference plane (single-ended S parameters), the propagation characteristics of differential and common-modes are determined. They are deduced directly from single-ended S parameters [Boc95]. In both cases, a 50 Ω reference impedance is considered. In the "S Parameter Analysis" window, mixed-mode S or Z parameters are plotted if the options "Mixed-mode S" or "Mixed-mode Z" are selected in the "Conversion" part of the screen.

Select "Mixed-mode S". In "Simulation data source" part", select the following parameters and click on the button 

to plot them:

- Sdd11: reflection coefficient of the differential-mode seen from the input of the cable
- Sdd12 : transmission coefficient of the differential-mode between the input and the output of the cable
- Scc11: reflection coefficient of the common-mode seen from the input of the cable
- Scc12 : transmission coefficient of the common-mode between the input and the output of the cable
- Sdc11: differential-mode to common-mode conversion at the input of the cable

The result is shown in Figure 3- 75. Sdd11 and Sdd12 parameter characterize the propagation of differential-mode through the cable, while Scc11 and Scc12 characterize common-mode. Sdc11 is equal to zero, such as Sdc12, Scd11 or Scd12: there is no conversion between differential-mode and common-mode because the modeled cable is symmetrical.

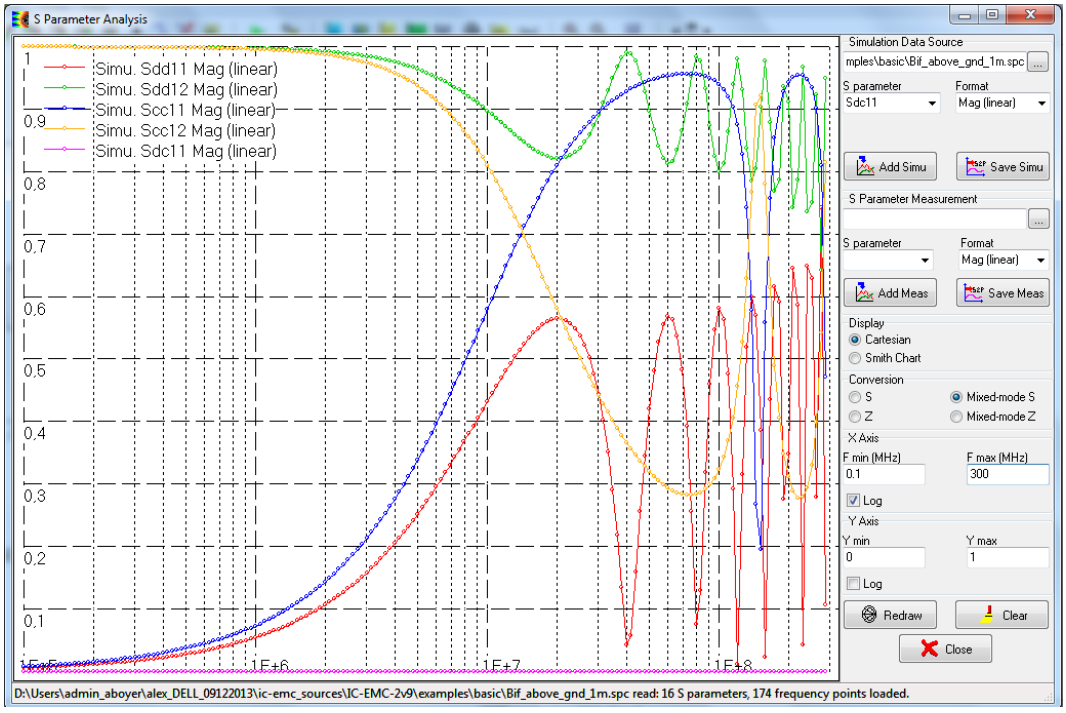


Figure 3- 75: Mixed-mode S parameter plot of a bifilar pair cable (\Examples\basic\Cables\ Bif_above_gnd_1m.sch)

III.9.3 Package modeling

IC-EMC proposes two tools based on two different approaches to build electrical models of IC package. The first method uses some dimensions about package provided by IBIS file to build a simple 3D geometrical model of the package and evaluate the stray resistance, inductance and capacitance of package pins from closed-form mathematical expressions. The second method reconstructs a more realistic 3D geometrical model of the package automatically or manually. The stray R, L, C elements are computed according to a PEEC method [Rue72].

III.9.3.1 Package model extraction from IBIS file

The module « Tools > Advanced Spice and IBIS » generates SPICE-compatible and IBIS-compatible netlists including the package parasitic R,L,C values for each package pin. This tool is also accessible from the IBIS interface (see part III.5). This tool saves the time of tedious data entry required in the more sophisticated three-dimensional programs that require large amounts of CPU time. This section describes the main features of the module.

III.9.3.1.1 Principles

The program builds a package layout by using the user-defined dimensions to generate approximate lengths and positions of the package's internal routing. The information required is the package type, pin pitch, pin list, package size and cavity size (Figure 3- 76). The information is listed using hidden keywords added to the [package model] section of the IBIS description.

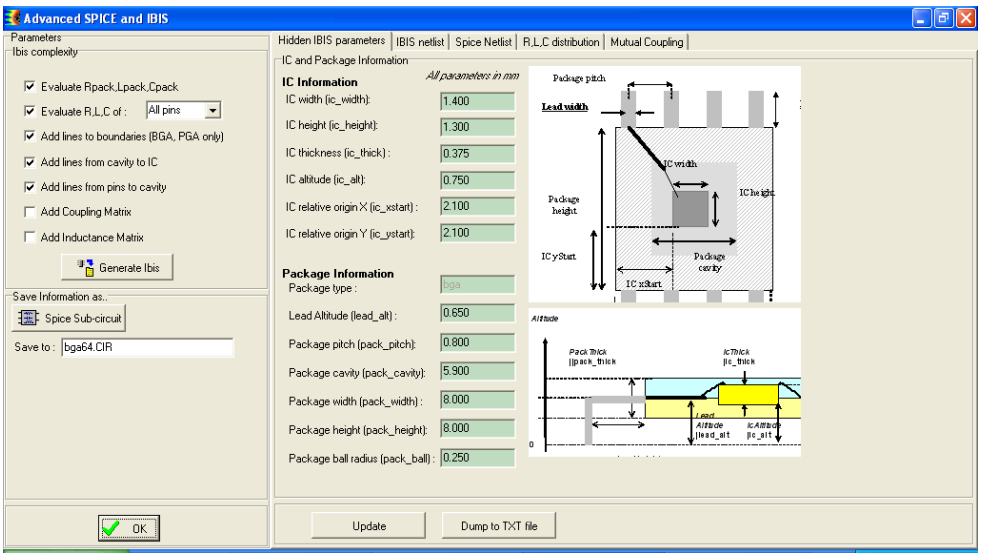


Figure 3- 76: Module "Advanced SPICE and IBIS" on a BGA (examples\ibis\BGA64.ibs)

The list of hidden parameters is described in Table 3- 7. The most important parameters appear in the main menu of the module, as can be seen in Figure 3- 76. Recall that the

hidden keyword information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders.

III.9.3.1.2 How stray R,L,C elements are computed

The tool first develops a 2D-geometric floorplan of the leads by calculating the length and position angle of the traces. The 2D view can be observed using the command “EMC > Ibis Interface” (Figure 3- 77).

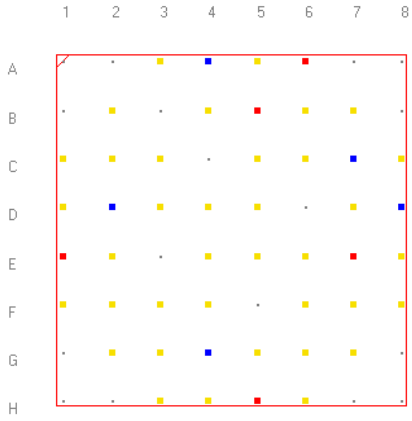


Figure 3- 77: 2D floorplan of a BGA 64 package (examples\ibis\BGA64.ibs)

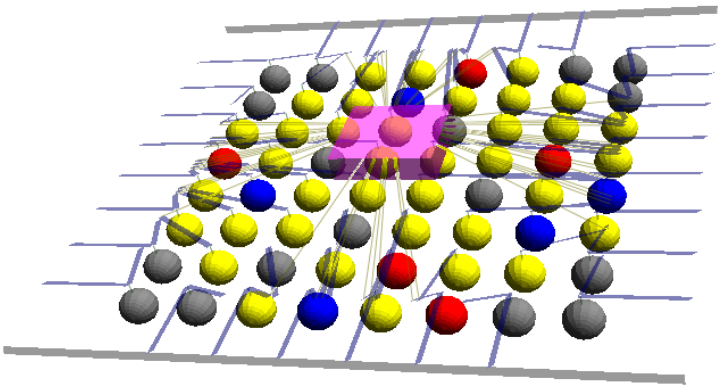


Figure 3- 78: 3D reconstruction of the BGA 64 (examples\ibis\BGA64.ibs)

Then, the program determines the trace structure, length and position in 3D. Figure 3- 78 shows the 3D reconstruction of the package. The view can also be obtained from “Tools > 3D Package Viewer”. To obtain reasonably accurate values for R,L and C, analytical formulations as described in section 3.3 – Conductor and Passive Models are employed. Each electrical parts of each wire (bonding, lead, soldier ball) is considered separately. For each elementary electrical wire, we compute:

- the resistance
- the self inductance;
- the capacitance to a ground plane

and optionally:

- the mutual inductance Lx with its nearest neighbors

- the mutual capacitance Cx with its next neighbor

In the BGA, each wire consists of 5 conductor parts, as illustrated in Figure 3- 79:

1. Ball
2. Ball to Via
3. Via
4. Via to Cavity
5. Cavity to boundaries
6. Cavity to IC

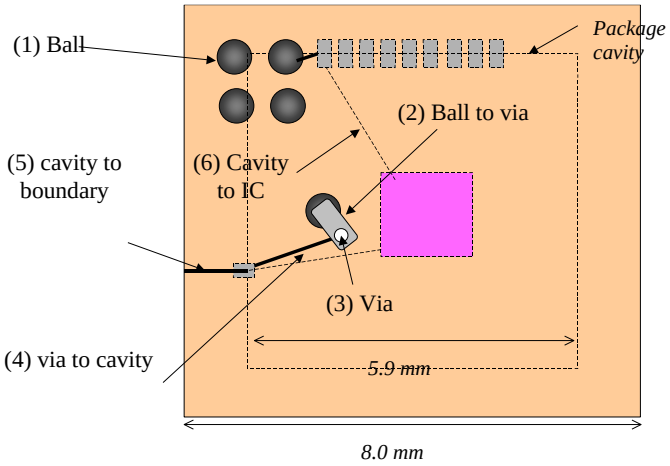


Figure 3- 79: The 6 electrical elements forming each pin of the BGA package

III.9.3.1.3 Stray R,L,C elements in IBIS file

In IBIS specification, the R,L,C values defined in the [Package] field, items R_pack, L_pkg, C_pkg are provided in a min/typ/max fromat. The tool “Advanced SPICE and IBIS” can determine the parasitic elements of the package in an IBIS compatible format as described in Figure 3- 80.

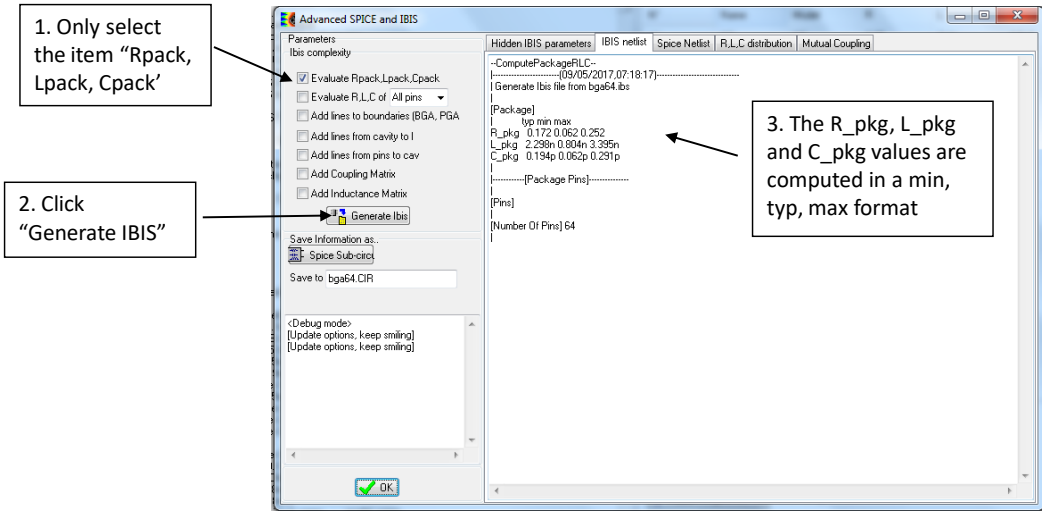


Figure 3- 80: Computing R_pkg, L_pkg and C_pkg in min,typ,max format (examples\ibis\BGA64.ibs)

III.9.3.1.4 Complete Ibis Netlist

Select the desired items in the “Ibis complexity” left menu, click “Generate IBIS”, and see the corresponding text in IBIS v6.1 format listed in the right menu “IBIS Netlist”. The text can be copy/paste. In the example shown in Figure 3- 81, the R,L,C parasitic information is added to each pin of the package in the [Pins] section. The values have been deduced from the 3D package reconstruction. The text can be used to update the IBIS file.

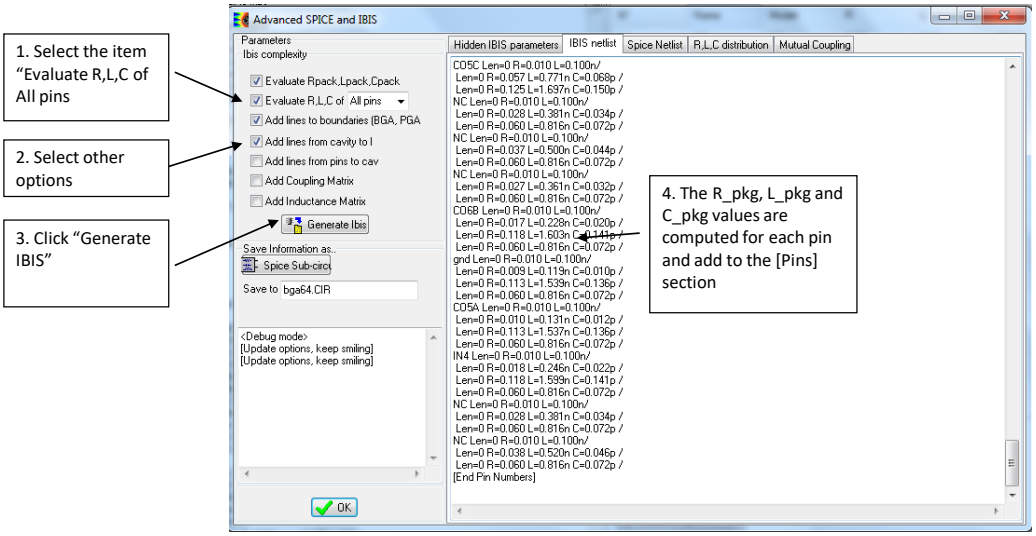


Figure 3- 81 : Add R_pkg, L_pkg and C_pkg information for each pin (examples\ibis\BGA64.ibs)

III.9.3.1.5 SPICE Netlist

The SPICE netlist contains the same information as for the IBIS netlist, but in a SPICE-compatible format. The syntax used to describe the netlist corresponds to a Sub-circuit (keyword SUBCKT). Note that all elements selected in the left menu “Ibis complexity” are described in SPICE format (Figure 3- 82). The subcircuit can be used as it in a larger SPICE simulation.

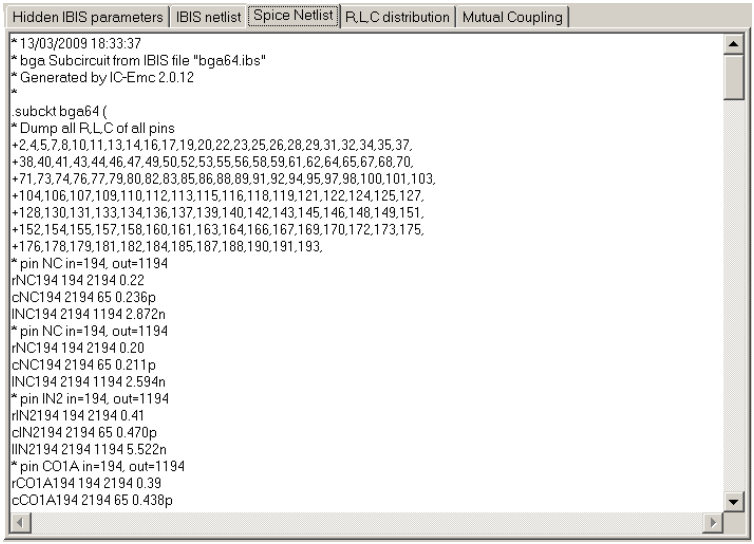


Figure 3- 82 : SPICE sub-circuit corresponding to the electric description of R,L and C (examples\ibis\BGA64.ibs)

III.9.3.1.6 R,L,C Distribution

The item « R,L,C » distribution is convenient to have a complete view of the inductance, capacitance and resistance values depending on the pin number. Mutual inductance and capacitance values are also computed and their distributed can be displayed. In Figure 3- 83, the variation of inductance is bounded by values around 1.2 nH for shortest wires (except one unconnected pin around 0.7nH) and 3.4 nH for the longest wires.

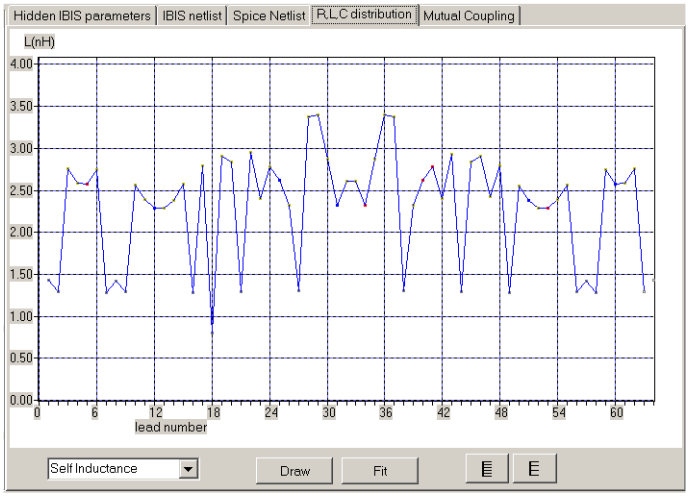


Figure 3- 83: Inductance variation versus lead number (examples\ibis\BGA64.ibs)

III.9.3.1.7 Inductance matrix in IBIS

In IBIS version 4.0 and above, the [Inductance Matrix] keyword enables to describe the mutual inductance coupling. Different format can be used for the [Inductance Matrix] data. The most concise format (Sparse_matrix) is used in IC-EMC.

The coefficients for Lij are defined as the voltage induced on conductor "j" when conductor "i"'s current is changed by 1 amp/sec and all other conductors have no current change. The [Inductance Matrix] is symmetrical. Therefore, only roughly one-half of the matrix needs to be described. By convention, the main diagonal and the UPPER half of the matrix are provided.

The notation [I, J] refers to the entry in row I and column J of the matrix. Note that I and J are allowed to be alphanumeric strings as well as integers. An ordering of these strings is defined in the [Pin Numbers] section.

The numeric entries of the matrices are standard IBIS floating point numbers. As such, it is permissible to use metric "suffix" notation. Thus, an entry of the L matrix could be given as 1.23e-9 or as 1.23n or 1.23nH.

From IBIS version 4.2, a Sparse_matrix is expected to consist mostly of zero-valued entries, except for a few non zeros. This feature is useful for PGA and BGA package coupling description. An N x N Sparse_matrix is specified one row at a time, starting with row 1 and continuing down to row N. Each new row is marked with the [Row] keyword. For the entry [I, J] of a row, it is necessary to explicitly list the name of pin J before the value of the entry is given. This specification serves to indicate to the parser where the entry is put into the matrix. Each (Index, Value) pair is listed upon a separate line. Consider the following example. Suppose that row 10 has nonzero entries [10,10], [10,11], [10,15], and [10,25]. The following row data would be provided:

```
[Row]   10
| Index        Value
10             5.7e-9
```

11	1.1e-9
15	1.1e-9
25	1.1e-9

Note that each of the column indices listed for any row must be greater than or equal to the row index, because they always come from the upper half of the matrix. As alphanumeric pin names are used in BGA and PGA, special care must be taken to ensure that the ordering defined in the [Pin Numbers] section is observed.

The list of inductance couplings (noted “Lx”) can be generated using the item “Mutual Coupling” and selecting the button “L Coupling” (Figure 3- 84).

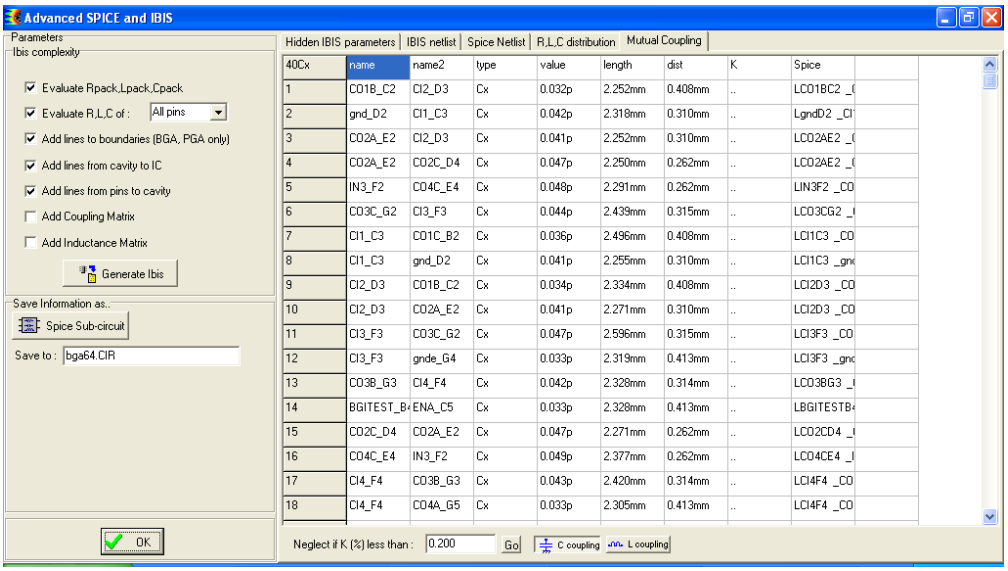


Figure 3- 84: Inductance coupling listed in IC-EMC (examples\ibis\BGA64.ibs)

III.9.3.1.8 Capacitance matrix in Ibis

The program computes the mutual capacitance of a conductor to all the other conductors that will contribute to its total capacitance. The total capacitance is the sum of the ground capacitance and all mutual capacitors calculated for that ball position except the two nearest neighbors on each side. The list of mutual couplings can be seen in Figure 3- 85.

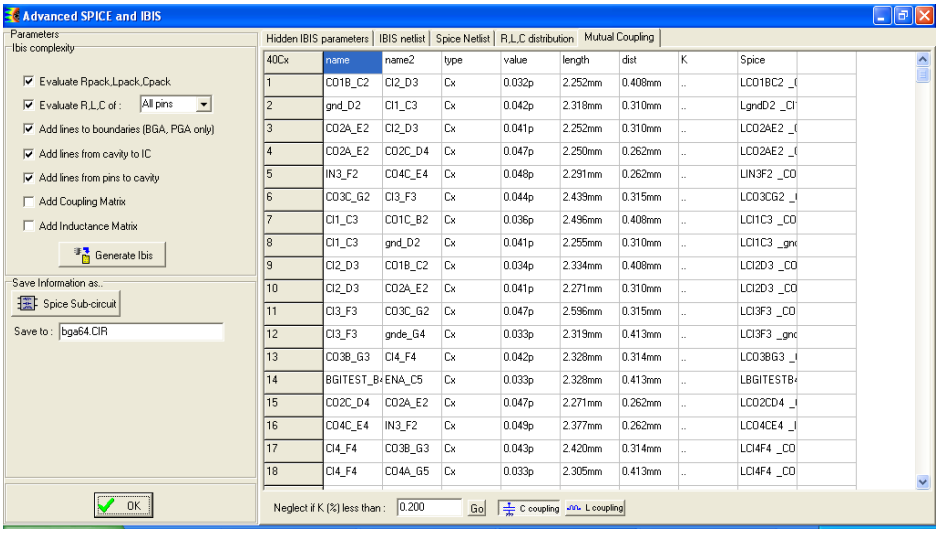


Figure 3- 85: Capacitance coupling listed in IC-EMC (examples\ibis\BGA64.ibs)

Values for the package material's dielectric constant and the thickness of the package are defined as hidden keywords in IBIS. The tool also calculates the capacitance to the ground plane. This is performed by using the conductor's length (l), width (w) and thickness (t), the effective dielectric constant of the package and the distance from the conductor to ground plane (H). The Delorme formulations are applied with theses data for all conductors [Del96].

A value for total capacitance is given to each conductor of the package which is the sum of all the conductor capacitance to the ground plane for each of the 5 elements. The Cij values are the coupling capacitances between adjacent leads. In IBIS, we use [Capacitance Matrix] for this description.

III.9.3.1.9 Resistance matrix in Ibis

Frequency dependent models of resistance cannot be inserted in IBIS. Consequently, the R matrix is computed at a user's defined frequency. It is recommended to fix that frequency to 100 MHz up to 10 GHz depending on the target simulation, as the resistance values are significantly higher that the DC values at such high frequencies

III.9.3.1.10 R,L,C matrix insertion in IBIS

The Keyword [Pin Numbers] not only indicates to the parser the set of names that are used for the package pins but also lists the R,L,C elements for each section of a pin's die to pin connection. Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as the number of pins given by the preceding [Number Of Pins] keyword. Each pin name is followed by a combination of *Len, R, L* and *C* sub-parameters (Table 3- 10).

Len	The length of a package stub section. Lengths are given in terms of arbitrary 'units'.
L	Inductance of each section, in henries/unit length. For example, if the total inductance of a section is 3.0nH and the length of the section is 2 'units', the inductance would be listed as L = 1.5nH (i.e. 3.0 / 2).
R	The DC (ohmic) resistance of a package stub section, in terms of ohms/unit length.
C	The capacitance of a package stub section, in terms of farads/unit length.

Table 3- 10: Keywords used to insert RLC matrix in IBIS file

A section description begins with the Len sub-parameter and ends with the slash (*/*) character. The value of the *Len, L, R*, and *C* sub-parameters and the sub-parameter itself are separated by an equals sign (=). If the *Len* sub-parameter is given as zero, then the L/R/C sub-parameters represent lumped elements. If the *Len* sub-parameter is non-zero, then the L/R/C sub-parameters represent distributed elements.

A three-section package stub description that includes a bond wire (lumped inductance), a trace (treated as a transmission line with DC resistance), and a pin modeled as a lumped L/C element is shown below:

```
|
[Pin Numbers]
A1 Len=0 L=1.2n/ Len=1.2 L=2.0n C=0.5p R=0.05/ Len=0 L=2.0n C=1.0p/
|
```

The [Inductance Matrix] and [Capacitance Matrix] are declared in the [Model Data] section that ends with [End Model Data]. The data is a set of three matrices: the resistance ©, inductance (L), and capacitance (C) matrices. Each matrix can be formatted differently.

III.9.3.2 Semi-automatic construction of a package model

The method presented in the previous part is adapted for a simple evaluation of package model, but the computed values are not accurate because of the approximate geometrical modelling of the package. In order to produce more accurate package model, a second method is proposed. This method is based on a more realistic geometrical model construction followed by a R, L, C extraction based on a Partial Element Equivalent Circuit (PEEC) algorithm [Rue72]. The PEEC method is a popular electromagnetic solving method adapted to coupling problems in electronic devices (cables, boards, circuits). This method is able to extract an equivalent passive circuit from an electromagnetic problem, so that electrical network simulators as SPICE can be used as solver.

III.9.3.2.1 Partial element theory and PEEC method

PEEC is based on the concept of partial elements, where each small elements of a conductor can be modeled by a partial element (a resistance, a self or mutual inductor, a capacitor or a mutual capacitor) that contributes to the total impedance of the conductor. Figure 3- 86 illustrates the concept of partial elements on a rectangular loop. Each side of the loop is decomposed in a partial resistance and inductance. Each partial self inductor of the loop are coupled with the other inductor by a mutual inductor.

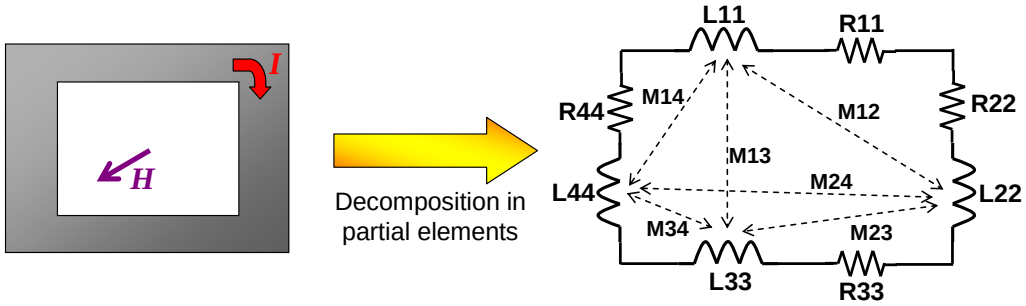


Figure 3- 86 : Decomposition in partial elements of a rectangular loop

Knowing the values of partial elements, the total resistance and inductance of the loop can be computed using equations III-10 and III-11. The total resistance is linked to the circulation of current along each partial element. The total inductance is linked to the flux of magnetic field through the loop surface so that it is equal to the sum of every self and mutual partial inductor.

$$R_{tot} = \sum_i R_{ii} \qquad \textit{Equ. III-12}$$

$$L_{tot} = \sum_i L_{ii} + \sum_i \sum_j M_{ij} \qquad \textit{Equ. III-13}$$

The PEEC method was developed in 1972 by A. Ruehli [Rue72] to analyze electrical interconnects with complex and arbitrary shapes. The principle is the conversion of each of physical structures (track, plane, substrate, via…) into equivalent passive model with localized R, L, C. PEEC method is not a full wave or exact electromagnetic method because it is based on the quasi-static approximation. This approximation simplifies the resolution of

Maxwell equations by assuming that wave propagation speed is infinite in a structure with a given length.

The PEEC method is based on the Electrical Field Integral Equation (EFIE) solving, presented in equation III-12. The total electric field is equal to the contribution of incident field Ei and scattering field Es induced by currents and charges on the structure.

$$\vec{E}_{tot} = \vec{E}_i + \vec{E}_s \qquad \textit{Equ. III-14}$$

From this equation, an equivalent passive circuit can be extracted with resistive, inductive and capacitive contributions. For each partial elements of the studied structure, the incident field is supposed to be null. The scattering electric field can be expressed with scalar and potential vectors as shown in equation III-13.

$$\vec{E}_{tot} = -\frac{\partial}{\partial t}\vec{A} - \vec{\nabla}V \qquad \textit{Equ. III-15}$$

Expressions of potentials are respected and equation III-14 is obtained. The total field induced by current and charges present at a point r' can be computed at any point r.

$$\vec{E}_{tot}(r,t) = -\frac{\partial}{\partial t}\left[\frac{\mu_r\mu_o}{4\pi}\int_V \frac{1}{|r-r'|}\vec{J}(r')dV\right] - \vec{\nabla}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r}\int_S \frac{1}{|r-r'|}q(r')dS\right] \qquad \textit{Equ. III-16}$$

The PEEC method is a numeric method so that the geometrical structure must be meshed in N elementary cells characterized by a volume Vi, a section Ai and lateral section Si. Equation III-14 can be rewritten in the following form:

$$\vec{E}_{tot}(r,t) + \sum_{i=1}^{N}\left[\frac{\mu_r\mu_o}{4\pi A_i}\frac{\partial I_i}{\partial t}\int_{Vi}\frac{1}{|r-r'|}dV_i\right] + \sum_{i=1}^{N}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r S_i}\vec{\nabla}q_i\int_{Si}\frac{1}{|r-r'|}dS_i\right] = \vec{0} \qquad \textit{Equ. III-17}$$

In order to determine the electromagnetic behavior of an elementary cell, the electric field is averaged on all the cell section with the following operator: $\frac{1}{A_j}\int_{Vj} dV_j$. Finally the previous equation can be written into:

$$\frac{1}{A_j}\int_{Vj}\vec{E}_{tot}(r,t) + \sum_{i=1}^{N}\left[\frac{\mu_r\mu_o}{4\pi A_i A_j}\frac{\partial I_i}{\partial t}\int_{Vj}\int_{Vi}\frac{1}{|r-r'|}dV_i dV_j\right] + \sum_{i=1}^{N}\left[\frac{1}{4\pi\varepsilon_o\varepsilon_r S_i S_j}\vec{\nabla}q_i\int_{Sj}\int_{Si}\frac{1}{|r-r'|}dS_i dS_j\right] = \vec{0} \qquad \textit{Equ. III-18}$$

The first term is the resistive contribution or the self resistor of the meshed partial element. The second term is the inductive contribution, containing the self inductance of the partial element and all the mutual inductances with other partial elements. The last term is the capacitive contribution, containing the potential of the partial element and the potential compared to the other partial elements. This equation is applied to every partial elements of the meshed structure which can be replaced by equivalent R, L, C circuits.

When the previous equation has been solved on each partial element, the complete structure can be modelled by an equivalent electrical circuit that can be solved with an electrical solver as SPICE.

III.9.3.2.2 Application to rectangular section conductors

Figure 3- 87 illustrates the meshing of two conductor adapted to the partial inductance computation. Each conductor is meshed in elementary cell along all its length, so that the current can flow through an elementary volume.

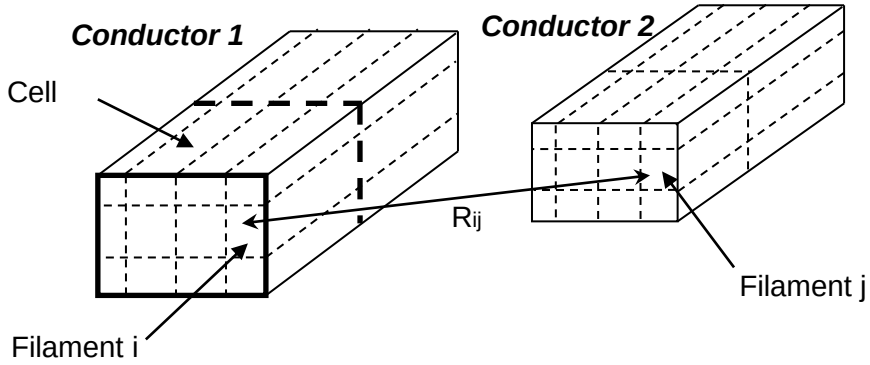


Figure 3- 87 : Meshing in elementary filaments of two conductors

From equation III-16, the inductive contribution can be isolated as described by equation III-17.

$$L_{12} = \frac{\mu_o}{4\pi A_1 A_2} \int_{cond\,1} \int_{cond\,2} \frac{l_1 \times l_2}{|r_1 - r_2|} dV_2 dV_1 \qquad \textit{Equ. III-19}$$

with:

- L_{12} : partial inductance between conductors 1 and 2
- A_1, A_2 : section of conductors 1 and 2
- li, lj: orientation of filament i and j
- R_{ij} : distance between meshes i and j
- dV_i, dV_j : elementary volumes between meshes i and j

The result of partial inductance extraction by PEEC method is given in the form of a partial inductance matrix. Self inductances are present in the diagonal of the matrix.

Figure 3- 88 illustrates the meshing of two conductors dedicated to the partial capacitor computation. Each meshed conductor is meshed along all its length in elementary cells. The lateral surface is meshed in elementary panels on which the total charge is spread.

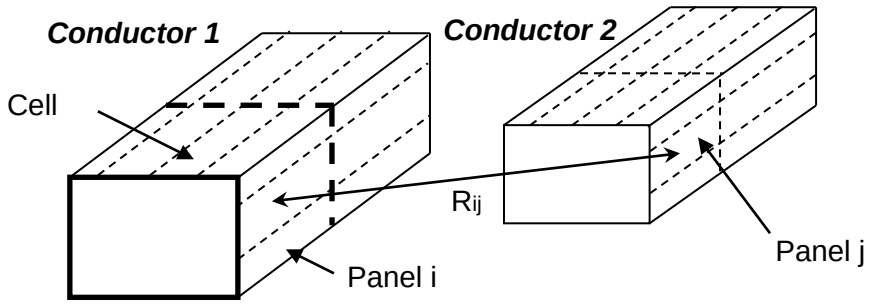


Figure 3- 88 : Meshing in elementary panels of two conductors

From equation III-16, the capacitive contribution can be isolated. However the expression does not directly give the partial capacitors but provides surface potential as described in equation III-18.

$$P_{12} = \frac{1}{4\pi\varepsilon S_1 S_2} \int_{cond\,1} \int_{cond\,2} \frac{1}{|r_1 - r_2|} dA_2 dA_1 \qquad \textit{Equ. III-20}$$

with:

- P_{12} : potential between conductors 1 and 2
- S_1, S_2 : lateral section of conductors 1 and 2
- R_{ij} : distance between panels i and j
- dA_i, dA_j : elementary surface of panels i and j

The result of equation III-18 is given in term of a potential matrix P. Capacitor matrix C is obtained by inverting the potential matrix, as shown in equation III-19.

$$[V] = [P][Q] \Leftrightarrow [C][V] = [Q]$$
$$[C] = [P]^{-1} \qquad \textit{Equ. III-21}$$

III.9.3.2.3 Implementation in IC-EMC for package model extraction

IC-EMC proposes a tool to build easily realistic geometrical model of package and compute accurately partial inductances, resistances and capacitors. Click “Tools > Advanced Package Model” to open this tool. This tool is composed of three parts for the definition of the geometrical model, the visualization of the 3D package geometric model and the computation of partial elements.

III.9.3.2.4 Package model construction

When the tool is opened, only the first page called “Package Generation” is visible. This page is dedicated to the construction of the package model. The tool proposed several types of standard package: Dual In Line (DIL), Small Outline Package (SOP), Quad Flat Package (QFP) and Ball Grid Array (BGA). The page is divided in two parts: on the right, numerous geometrical information are proposed to build the geometrical model, reported in Figure 3-90.

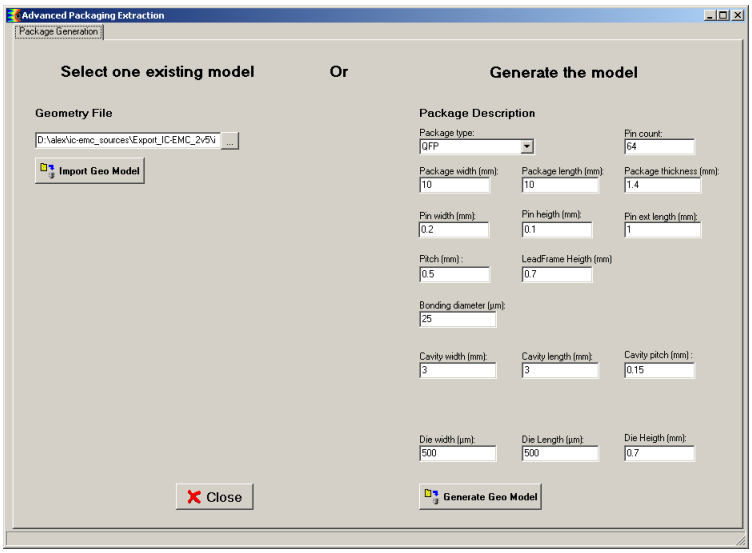


Figure 3- 89 : Interface to define realistic package model ("Tools > Advanced Package Model")

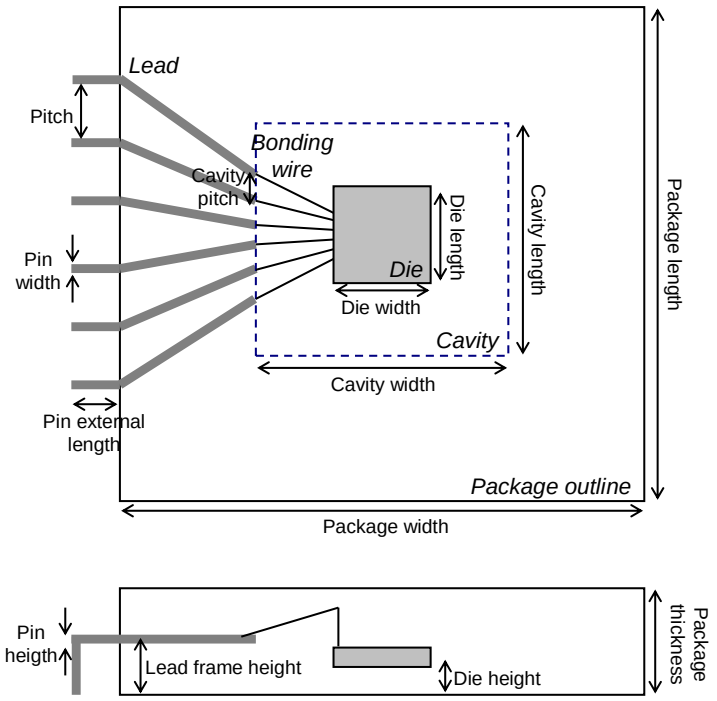


Figure 3- 90 : Interface to define realistic package

Click on the button “Generate Geo Model” to build the geometrical model, which is saved in a specific file with .geo extension. Only DIL, SOP and QFP are automatically generated. BGA are complex multilayer package and the internal routing cannot be automatically reconstructed. If BGA type is selected and you click on Generate Geo Model, a new window is opened to help the user to manually define the internal routing of the BGA.

The left part of the screen is simpler and is dedicated to the import of an existing GEO file previously generated. When the GEO file is correctly imported, the two other pages become visible. Import the file “examples\package\TQFP64.geo” and click on the button “Import Geo Model”. Open the page “Model Viewer” to see the geometrical model of the package (Figure 3- 91). The different leads, bonding wires and the die are placed.

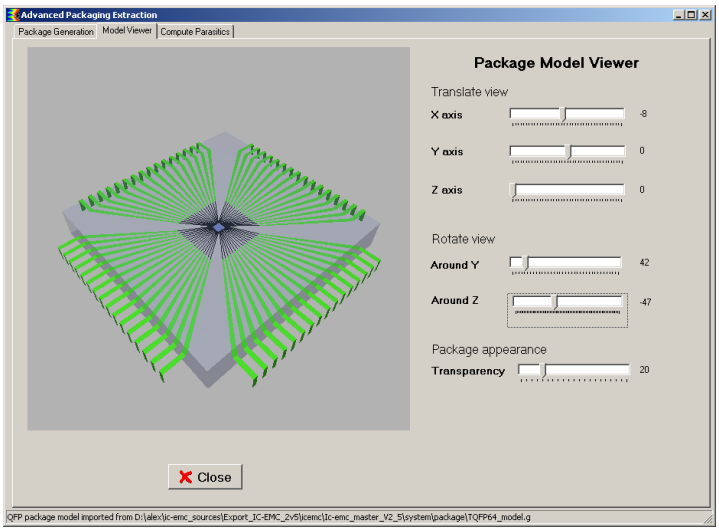


Figure 3- 91 : Display of a reconstructed 3D package model of a TQFP 64 (examples\package\TQFP64.geo)

III.9.3.2.5 Package partial element extraction

Open the page “Compute Parasitics” to compute the partial elements of package leads and bonding wires. Figure 3- 92 presents the screen.

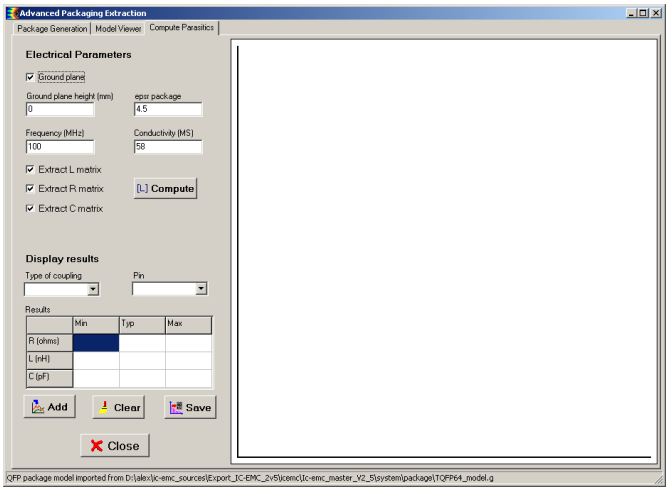


Figure 3- 92 : Interface to compute the partial elements of a package

First configure the electrical parameters of the computation. A perfect ground plane is placed under the package if the box "Ground plane" is checked. The dielectric constant epsr package of the package is set to 4.5, typical of a plastic package. As the simulator does not take into account dielectric materials, three options are proposed to approximate the effective dielectric constant:

- Free space: the dielectric constant of the space is constant and equal to epsr package
- Microstrip line: the lead are considered as microstrip line, an effective dielectric constant is computed from the height of the substrate, the width of the lead and epsr package
- Burried line: the lead is buried in the substrate, an effective dielectric constant is computed from the height of the substrate, the width of the lead and epsr package

Set the conductivity of the conductors and the maximum frequency of the computation in order to compute the partial resistance and take into account skin effect. Finally, select the partial element types that you want to compute; R, L or C, and click on the button “Compute”.

The simulation takes several seconds, an advancement bar appears to indicate the remaining time before the end of the simulation. At the end of the simulation, the field “Type of Coupling” and “Pin” are filled and you can select the type of partial elements that you want to display. Click on the button Add to display partial elements for every pins of the package on the graph of the right part of the screen. Figure 3- 93 presents the simulated partial self inductance and capacitance for the TQFP64 package.

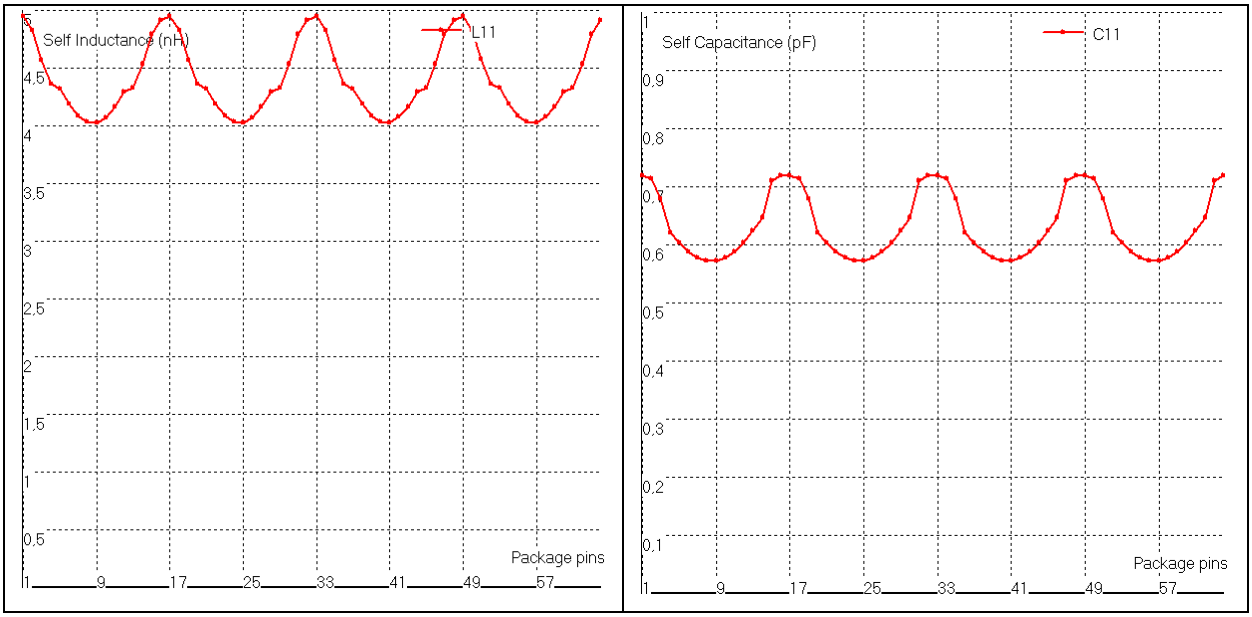


Figure 3- 93 : Simulation of the partial self inductance (on the left) and capacitance (on the right) (examples\package\TQFP64.geo)

The different simulated partial elements are exported in .L, .R and .C file for partial inductances, resistances and capacitances respectively.

III.9.3.2.6 BGA model construction

BGA geometrical model cannot be automatically generated. That’s why IC-EMC proposes an interface to help the user to build manually the geometrical model. Return to the first page of the Advanced Package Extraction tool and enter the different mechanical parameters of the package. Click on “Generate Geo Model” to create a new Geo model or “Modify Geo Model” to modify an existing Geo model.

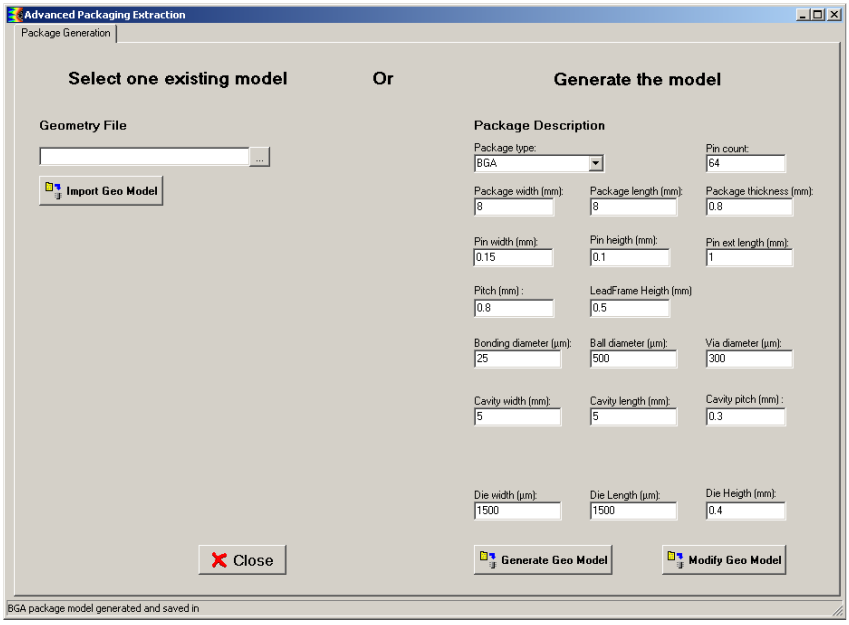


Figure 3- 94 : Launch the BGA model manual construction

An open dialog window asks for a .geo file. Then the following screen appears. This screen defines the number of the internal routing layers in the BGA, the characteristics of the tracks for each layer, and the number and characteristics of embedded dies. Click Add layer to add a new layer and change directly in the tables the different value.

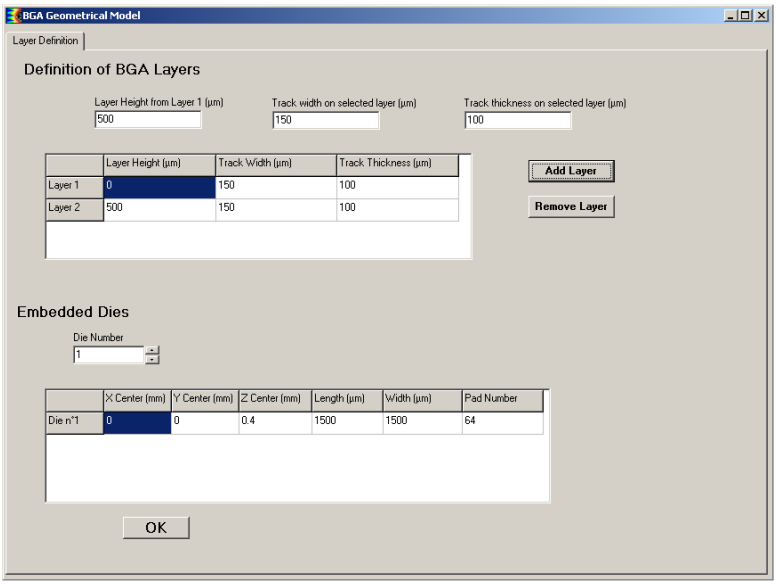


Figure 3- 95 : Definition of the BGA internal layers and the number of dies

When the layer and the die information are set, click on the button “OK” to start the manual design of the internal routing of the BGA. A new page called “BGA design” becomes visible, described in Figure 3- 96 left. The 3D screen is empty, if you change the visible layer to the Layer 2, the die becomes visible. Balls and bonding wires can be accurately automatically placed. Click on the button “Ball Placement”, the balls appear on the screen. The button “Bonding Placement” also appears. Click on this button and all the bonding wires are placed, as shown in Figure 3- 96 right.

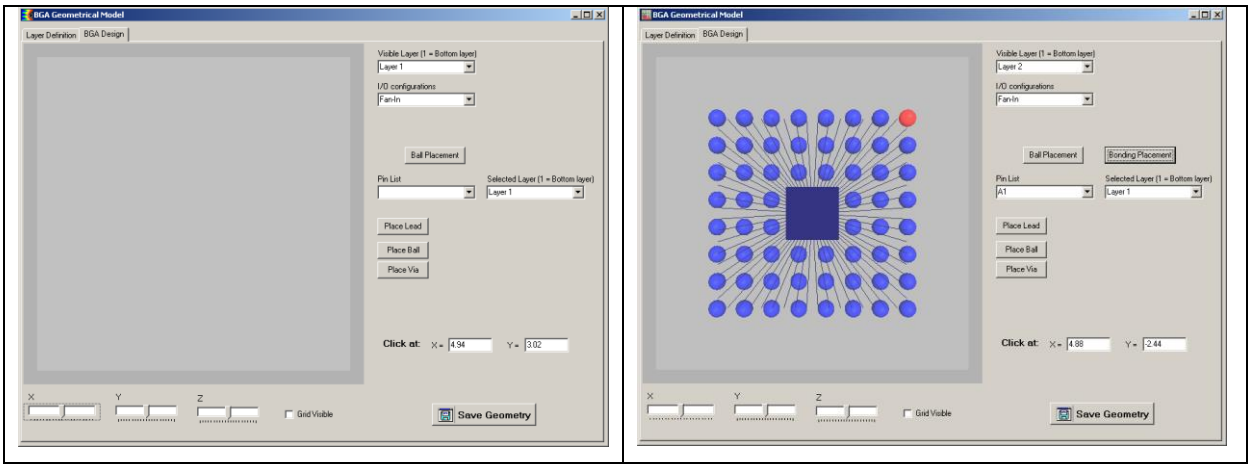


Figure 3- 96 : Empty BGA design screen (on the left) and automatic placement of balls and bonding wires (on the right)

The red ball indicates the selected pin from which you can start the pin design. With the field, you can define on which layer you can design a new element of pin design. Three elements can be design: a lead, a ball or a via. Click on one button “Place Lead”, “Place Ball” or “Place Via”. Push the left button of the mouse to place the first point of the new element (e.g. a lead) and release the mouse to indicate the last point of this element. A yellow shape indicates the new elements. Finally, click on the button “Validate” to confirm the placement of a new element.

Let’s design the pin number 1 starting from the ball. Select A1 in “Pin List” field and Layer 1 in “Selected Layer”. Place a lead on the first layer. Then place a 300 µm wide via between first and second layers. Finally, place a lead on the second layer that connects the extremity of a bonding wire. The connected bonding wire becomes red, indicated that this bonding wire is now associated to pin 1. Figure 3- 97presents the final result.

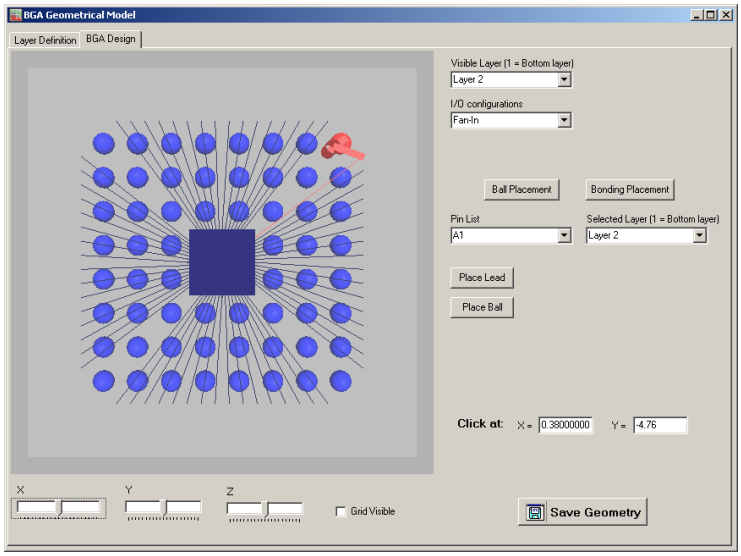


Figure 3- 97 : Design of pin A1 (examples\package\test_BGA.geo)

Do the same for all the pins of the package. At the end, click on the button “Save Geometry”. The screen is closed and you return to the Advanced Package Extraction Tool to view the geometrical model and compute electrical partial elements. In order to present an example of a complete BGA model built with this tool, open the file

"examples\package\BGA64_model.geo". This file describes the full geometrical model of the BGA 64 package. Figure 3- 98 presents the geometrical model. The internal routing of the BGA was built from a X-ray view of the package. Figure 3- 99 presents the simulation result of the partial inductance : the distribution of self inductance values according to pin position is displayed. This distribution can be compared with the distribution shown in Figure 3- 83, computed with the tool "Advanced SPICE and IBIS" from a basic geometrical model built from IBIS file. Both methods provide the same inductance range (between 2 and 3.5 nH per pin).

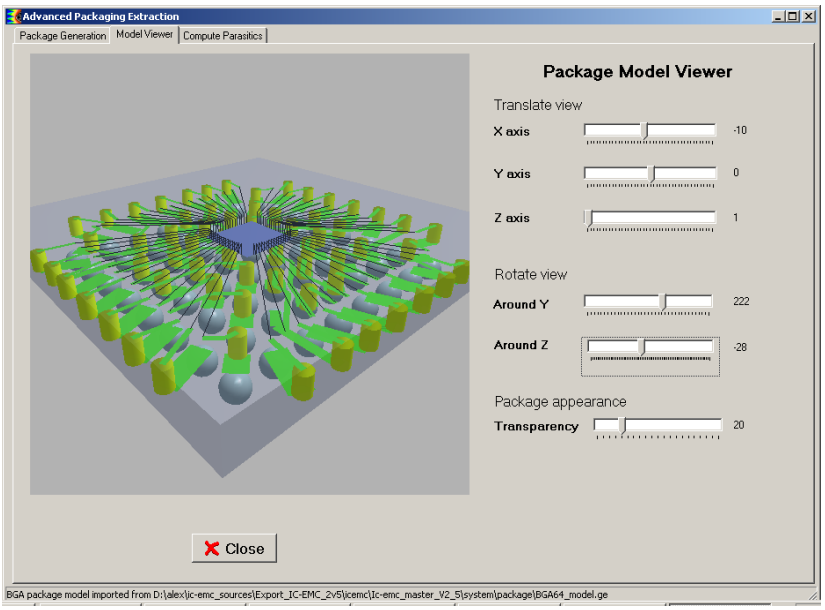


Figure 3- 98 : Constructed model of a BGA 64 (examples\package\ BGA_model.geo)

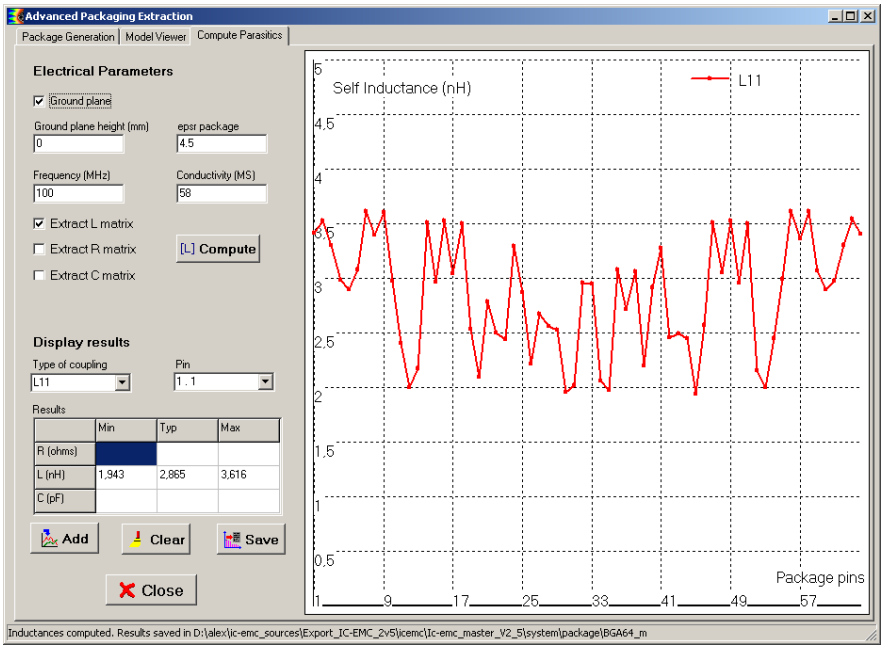


Figure 3- 99 : Simulated partial inductance of a BGA 64 (examples\package\ BGA_model.geo)

III.9.4 Modeling of a rectangular power-ground plane pair

In multilayer PCBs, the inner layers are often entirely taken up by solid planes forming power and ground planes for DC power distribution to circuits. Two adjacent power and ground planes (PG plane pair) form a 2D transmission line but, contrary to narrow traces, this line does not propagate a TEM wave along the direction of the trace. This parallel-plate waveguide structure actually propagates a transverse magnetic (TM) wave in a 2D plane. This structure is characterised by a large number of parallel-plate waveguide modes whose resonant frequencies depend on plane geometry and separation. Due to the highly resonant behaviour of this structure, a PG plane pair constitutes a good coupling path for noise produced by circuits, which is propagated over the whole PCB and radiated from the board's edges. Numerous problems, such as power or signal integrity, conducted and radiated emission or immunity, are related to the design of the power distribution network.

The determination of the resonance mode of such structure usually requires numerical electromagnetic solver. However, for rectangular PG plane pair, formulations can be derived based on the 2D resonant cavity model. The tool "PG Plane Model" proposes an interface to define the geometry of a PG power plane, the position of access ports and the extraction of Z, S or Y parameters between the access ports. Finally, an equivalent electrical model of the structure can be derived.

III.9.4.1 Brief description of the 2D resonant cavity model

The 2D resonant cavity model is a frequency domain model. It considers a simple plane shape and an electrically short separation between planes. Here, only rectangular planes will be considered. The geometrical model is presented in Figure 3- 100. As separation distance h is negligible compared to the wavelength, the distribution of electric and magnetic fields within the cavity is independent of z, resulting in a 2D problem depending only on the x and y coordinates. Solving the Helmholtz equation gives their distribution. When the cavity is excited on a point or "port", the Helmholtz equation can be solved analytically as described in numerous publications such as [Lei95].

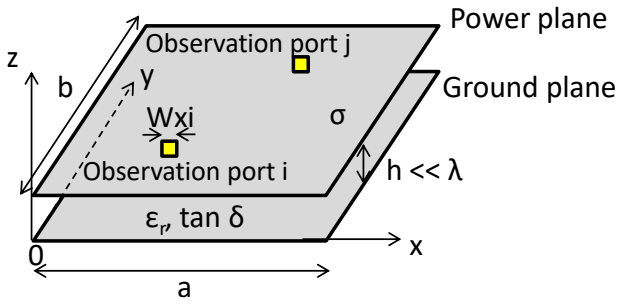


Figure 3- 100 : Rectangular 2D cavity formed by a PG plane pair

The field distribution within the cavity results from the superposition of an infinite number of transverse magnetic T_{Mmn} propagation modes characterised by an index pair (m,n). Equation I-20 gives the expression of the impedance Z_{ij} between ports i and j at frequency f. For i = j, Z_{ij} gives the input impedance seen at this port, but for other values, the transfer impedance between these ports is considered. The evaluation of impedance Z_{ij} requires a double infinite summation of all these modes. A mode (m,n) actually only becomes influential above its resonant frequency F_{Cmn} given by equation I-21, so only a limited number of modes contributes to the impedance at a given frequency. The number of terms to be summed is usually chosen *ad hoc* in order to reach convergence. The terms m and n are also called the orders of the model.

$$Z_{ij}(f)=\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{N'_{mni}N'_{mni}}{\frac{1}{j\omega L_{mn}}+j\omega C_{mn}+G_{mn}} \qquad \textit{Equ. III-22}$$

$$F_{Cmn}=\frac{1}{2\pi}\frac{1}{\sqrt{\varepsilon\mu}}\sqrt{\left(\frac{m\pi}{a}\right)^2+\left(\frac{n\pi}{b}\right)^2} \qquad \textit{Equ. III-23}$$

The different terms of the Zij expression are defined below. δ and tand are the skin depth and the loss tangent of the insulator material at frequency f respectively. The terms L_{mn}, C_{mn} and G_{mn} are equivalent to inductance, capacitance and conductance.

$$N_{mni}=\cos\left(\frac{m\pi x_i}{a}\right)\cos\left(\frac{n\pi y_i}{b}\right)\sin c\left(\frac{m\pi W_{xi}}{2a}\right)\sin c\left(\frac{n\pi W_{yi}}{2b}\right) \qquad \textit{Equ. III-24}$$

$$L_{mn}=\frac{h}{2\pi F_{Cmn}ab\varepsilon} \qquad \textit{Equ. III-25} \qquad C_{mn}=\frac{ab\varepsilon}{h} \qquad \textit{Equ. III-26}$$

$$G_{mn}=\frac{ab\varepsilon}{h}2\pi F_{Cmn}\left(\tan d+\frac{1}{h}\frac{1}{\sqrt{\pi F_{Cmn}\mu\sigma}}\right) \qquad \textit{Equ. III-27} \qquad N'_{\mathrm{mni}}=C_mC_nN_{mni} \qquad \textit{Equ. III-28}$$

$$C_m,C_n=\begin{cases}1 & if\ m,n=0\\ \sqrt{2} & otherwise\end{cases} \qquad \textit{Equ. III-29}$$

Equation I-20 shows that the cavity can be modeled as a series combination of an infinite number of cells formed by parallel equivalent inductance L_{mn}, capacitance C_{mn} and conductance G_{mn} [Na02]. Each cell is associated with one particular mode (m,n), where L_{mn} and C_{mn} model the storage of magnetic and electrical energy respectively, while G_{mn} models the conductor and dielectric losses. The contribution of a mode to the impedance between ports i and j depends on variables N'_{mni} and N'_{mnj}. An equivalent electrical model is derived from this expression and is shown in Figure 3- 101**Erreur ! Source du renvoi introuvable.**. Variables N'_{mni} and N'_{mnj} are modelled as an ideal transformer with a turns ratio of N'_{mni}:1 and N'_{mnj}:1.

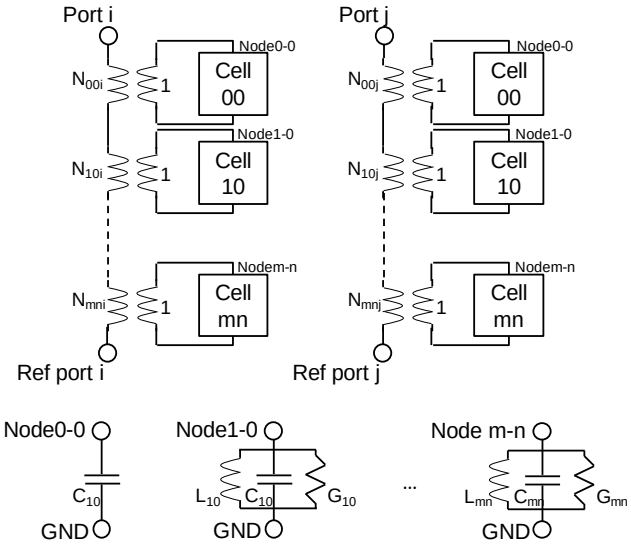


Figure 3- 101 : Equivalent electrical model of a rectangular 2D cavity formed by a PG plane pair

III.9.4.2 Open the tool "Cavity Model of PCB Power Planes"

Click on the menu "Tools > PG Plane Model" to open an interface dedicated to the modeling of rectangular PG plane pair. Its purpose is the computation of Z, S or Y parameters between several ports placed between the power and the ground planes and the extraction of an equivalent electrical circuit based on the 2D resonant cavity model. Figure 3- 102 presents the interface of the tool. The left part of the screen includes all the command to define the model and configure the result's display. The right part of the interface is blank initially. The simulated Z, S or Y parameters will be displayed on the screen.

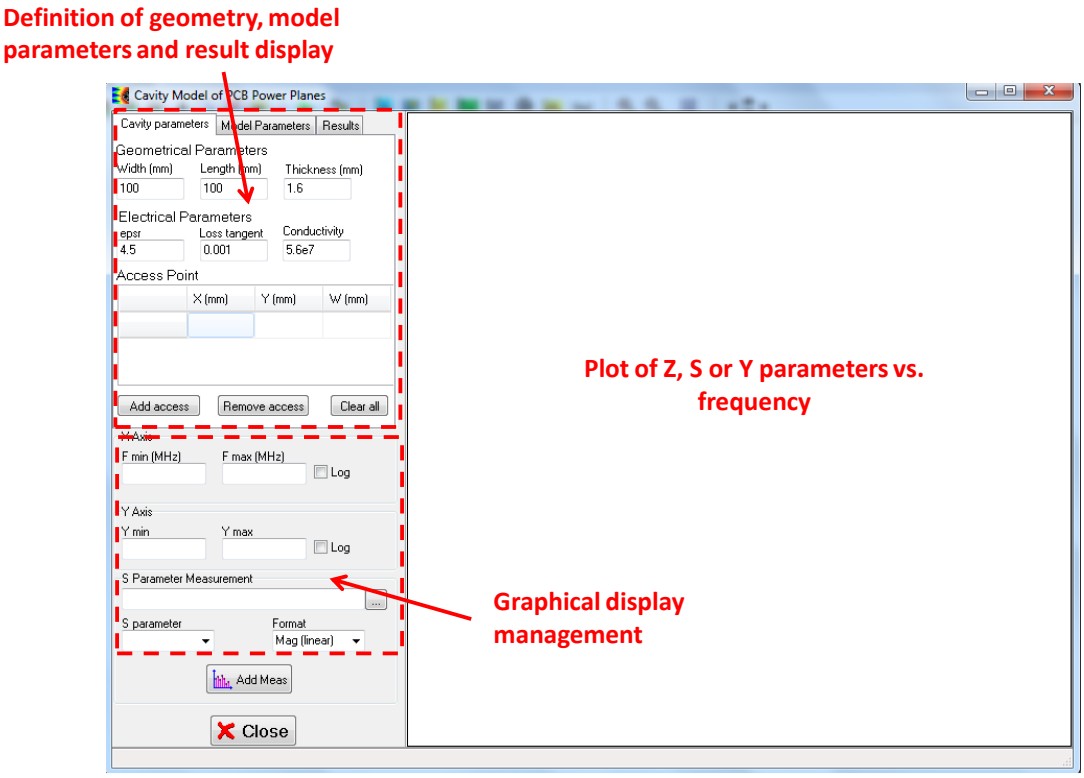


Figure 3- 102 : Interface for PG plane pair modeling ("Tools > PG Plane Model")

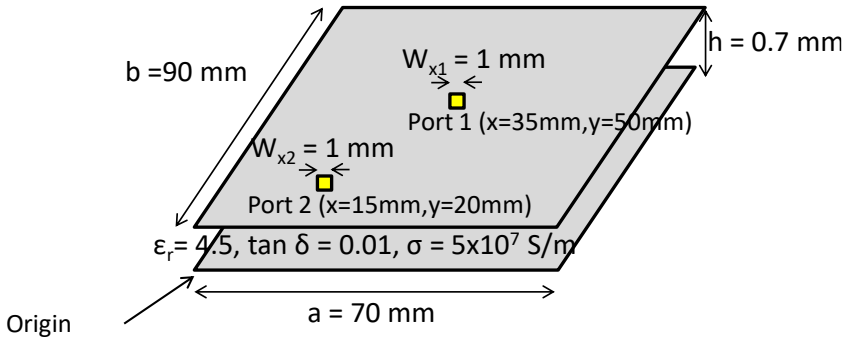
The upper left part of the screen presents three tabs for the three main operation of the modeling process:

- Cavity parameters: definition of geometrical and electrical parameters of the PG power plane pair, position of the ports
- Model parameters: definition of cavity model parameters (maximum order and frequency range), launching of the simulation
- Results: Selection of parameters to be displayed, export of the simulated Z, S or Y parameters, extraction of an equivalent electrical circuit

III.9.4.3 Build the geometrical model

In the following parts, we consider the following rectangular PG plane pair. The dimensions of the planes are given. They are supposed to be made with copper and separated by a FR4 insulator. The two ports may correspond to the position of a power pin of an IC which excites the PG plane pair (port 1) and a measurement point (port 2). Both ports are supposed to be a

1 mm wide square. All the ports are referenced to the ground plane. The (X;Y) position of the ports are defined according to an origin point placed on lower left corner of the plane.



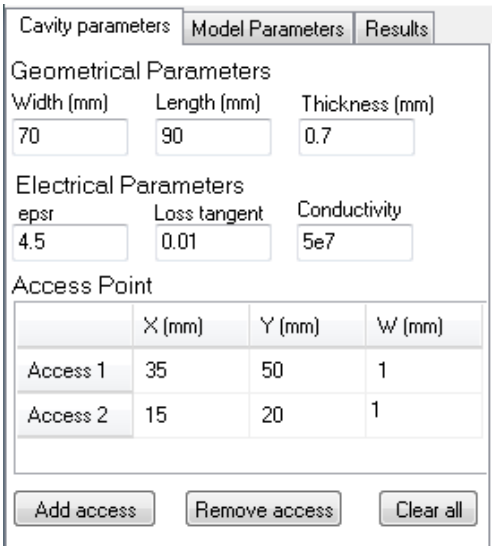


Figure 3- 103 : Studied power-ground plane pair (top); Geometrical and electrical parameters defined in the tool" PG Plane Model" (bottom)

The geometrical and electrical parameters of the PG plane pair are defined in the tab "Cavity parameters" as described in Figure 3- 103. To define a new port, type the X and Y coordinates of the port and its width (W) in the table Access Point. Then click on the button "Add access". The name of the ith port appears (Access i) if it is valid.

III.9.4.4 Computation of Z parameters

Once the geometrical model has been defined with its electrical parameters, the parameters of the computation have to be defined. The accuracy of the simulated Z, S or Y parameters depends on the orders m and n, at the price of a longer simulation time. With m or n equal to 50 to 100, a good compromise between accuracy and simulation time may be found. It is advised to start with small order values, increase them and verify that the result has converged to ensure that the choice of orders is proper. The frequency range and the number of frequencies have also to be defined, as shown in Figure 3- 104 : Configuration of the simulation. Finally, click on the button "Compute Model" to launch the computation of Z, S or Y parameters.

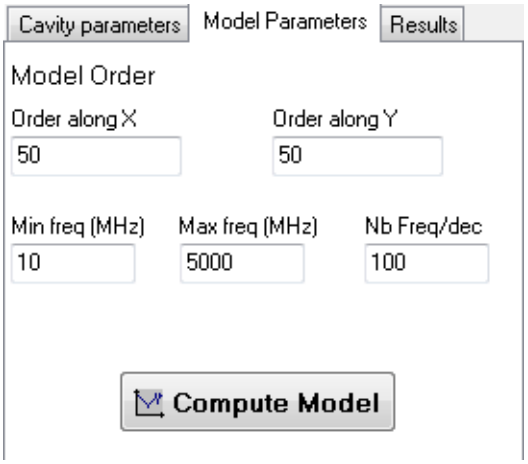


Figure 3- 104 : Configuration of the simulation

At the end of the computation, the message "Impedance between access ports have been successfully computed". Open the tab "Results" to select the parameters to be displayed: in the box "Parameter", select Z11, Z22 and Z12 successively and click on the button "Add" to display these Z parameters. They are plotted on the screen on the right. The bottom left part of the screen is dedicated to the axis settings. Configure a log-log X-Y axis to observe the evolution of Z parameters over several decades of frequency. Figure 3- 105 presents an example of result. Z parameters follow a complex evolution in frequency domains, with numerous resonance and antiresonance associated with the different TM propagation modes.

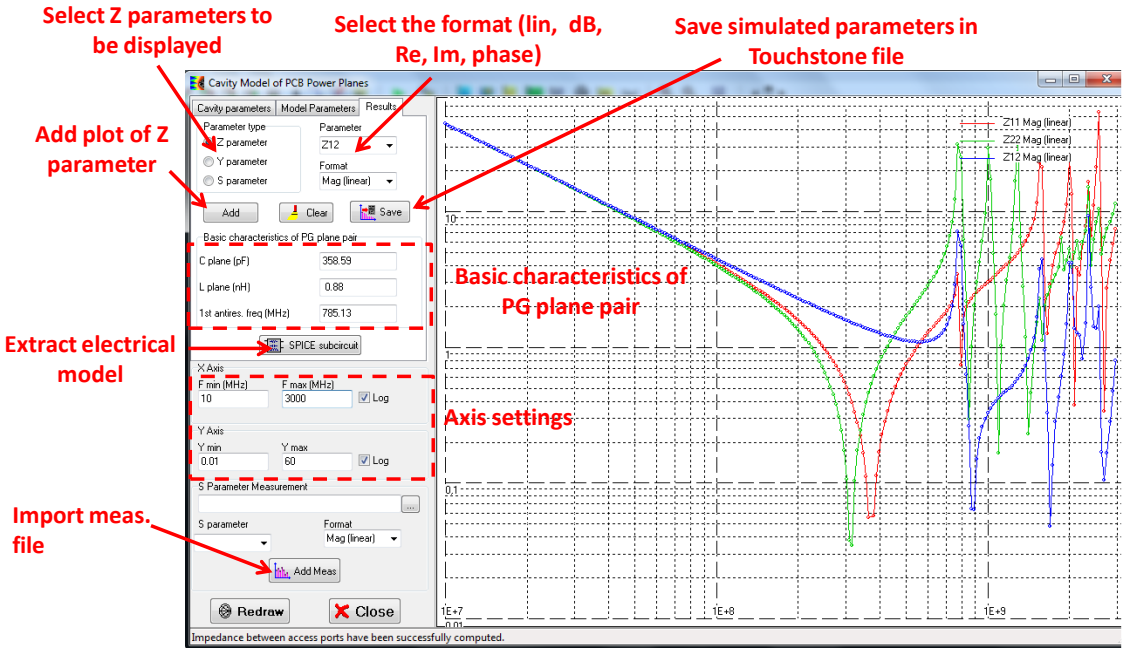


Figure 3- 105 : Display the simulated Z parameters between both access ports

Some basic characteristics of the PG plane pair are given in the part "Basic characteristics of PG plane pair":

- "C plane (pF)" gives the equivalent capacitance between power and ground planes
- "L plane (nH)" gives the total inductance forming by both planes
- The structure is characterized by several propagation modes with different resonant frequencies (see equation III-21). "1st antires freq. (MHz)" gives the resonant frequency of the

(1;0) mode i.e. the first antiresonance frequency that affects the system. This frequency is of primary importance since this antiresonance may induce serious voltage bounce on power supply delivery network.

The first antiresonance frequency is 785 MHz. At this frequency, impedance profiles exhibit local maxima. The simulated Z, S or Y parameters can be saved in a Touchstone file by clicking on the button "Save".

III.9.4.5 Extraction of an equivalent model

Tuning an equivalent electrical model from this impedance profile may be a complex and tedious task. However, due to the structure of the impedance equation (equation III-20), an electrical RLC circuit can be easily extracted (Figure 3- 101). Click on the button 

to save this equivalent circuit in a SPICE compatible subcircuit. The model is saved in a .sym symbol file ("examples\basic\PCB\PG_plane_pair.sym"). This symbol can be included on a schematic with command "Insert > User symbol (.SYM)". The symbol is shown in Figure 3- 106. It includes two ports made of a pair of two terminals : P_i is connected to the power plane at the i^{th} port, while Ref_i is connected to the ground plane at the i^{th} port.

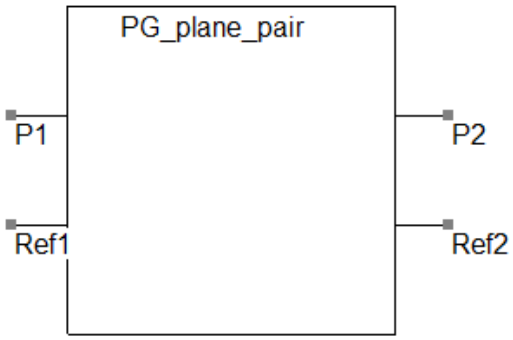


Figure 3- 106 : SPICE subcircuit of the PG plane pair

This symbol may be included in a SPICE model for AC or transient simulations.

III.10 ICEM model expert

The main objective of the ICEM-CE standard (Integrated Circuit Emission Model for Conducted Emission) [ICEM] is to propose a general framework for modelling the parasitic emission of analogue or digital integrated circuits in conducted mode. The ICEM-CE model mainly targets the switching of logic cores (CPUs)—with a focus on the power delivery network—and of input/output buffers, which are the main contributors to conducted noise.

From basic technological information about an integrated circuit available at early design stage, such as CMOS technology node, number of gates, die size, type of package, etc…, dynamic current consumption and IC interconnects can be evaluated and a first-order ICEM model can be derived for emission prediction purpose. This is the purpose of the ICEM Model Expert tool, available in the menu "Tools > ICEM Model Expert". Although the derived model cannot reach the same accuracy than a model built from post-layout information or measurements from a circuit, it can help IC or PCB designer to obtain a rapid evaluation of the expected emission level before design and fabrication, anticipate risks of non-compliance and analyze the influence of EMI mitigation techniques (number of supply pairs, package change, increase of on-chip decoupling, etc…).

ICEM Model Expert tool is described in the application note [ICEM_EXP] with a practical example done on a 32-bit microcontroller.

III.11 References

[IEC62-4]	IEC 62132-4 – edition 1.0: Integrated circuits - Measurement of electromagnetic immunity - Part 4: Direct RF power injection method, 2006-02-21.
[IEC61-4]	IEC 61967-4
[Boy08]	A. Boyer, E. Sicard, M. Fer, L. Courau, “Electrical Characterization of a 64 Ball Grid Array Package”, EMC Europe 2008 (EMC Europe 2008), Germany, 8-12 Sept. 2008.
[IBIS15]	IBIS I/O Buffer Information Specification - https://ibis.org/ver6.1/ver6_1.pdf - Ratified September 11, 2015.
[IEC61-3]	IEC 61967-3, “Methods of Radiated Emission – Surface Scan Method”, Technical Specification, International Electrotechnical Commission, Geneva, Switzerland, March 2002
[IECTR61]	IEC/TR 61967-1-1 Ed. 1.0, " Integrated circuits - Measurement of electromagnetic emissions - Part 1-1:General conditions and definitions - Near-field scan data exchange format.", Technical report, 2009-10-23, IEC.
[App_NF]	A. Boyer, " Prediction of the near field radiated emission of basic transmission lines", IC-EMC Application notes, 2012, www.ic-emc.org.
[App_PA]	C. Dupoux, S. Akue Boulingui, E. Sicard, "3G power amplifier case study", IC-EMC Application notes, 2011, www.ic-emc.org.
[Dup09]	C. Dupoux, S.I Akue Boulingui, E. Sicard, S.Baffreau, N. Bouvier, “Measurement and Simulation of Electromagnetic Interference in 3G Mobile Components”, EMC Compo 09, Toulouse, Nov 2009.
[Boc95]	D. E. Bockelman, W. R. Eisenstadt, "Combined Differential and Common-Mode Scattering Parameters: Theory and Simulation", IEEE Trans. on Microwave Theory and Techniques, vol. 43, no 7, July 1995.
[Rue72]	A. E. Ruehli, « Inductance Calculations in a Complex Integrated Circuit Environment», IBM Journal of Research and Development, Sept.1972.
[Del96]	N. Delorme, M. Belleville, J. Chilo, « Inductance and capacitance analytic formulas for VLSI interconnects », Electronic Letters, vol. 32, no. 11, 23rd May 1996,.
[ICEM]	IEC62433-2 - EMC IC modelling – Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE) - Ed. 1.0, Oct. 2008, IEC.
[ICEM_EXP]	E. Sicard, " ICEM Model Expert – Application to TC1796", IC-EMC Application Notes, www.ic-emc.org.
[Lei95]	G. T. Lei, R. W. Techentin, P. R. Hayes, D. J. Schwab, B. K. Gilbert, "Wave Model Solution to the Ground/Power Plane Noise Problem", IEEE Trans. on Instrum. and Meas., vol. 44, no 2, Apr. 1995.
[Na02]	N. Na, J. Choi, M. Swaminathan, J. B. Libous, D. P. O'Connor, " Modeling and Simulation of Core Switching Noise for ASICs", IEEE Trans. on Adv. Pack., vol. 25, no 1, Feb. 2002.

IV. Description of the menus

IV.1 Overview of the menus

Figure 4- 1 to Figure 4- 6 present the different IC-EMC menus. Some of these commands are also accessible through the icons in the command bar. The File menu is used to save and open IC-EMC electrical schematics, open an IBIS file (.ibs), open a technology file (.tec), save a subcircuit file (.sym), print or exit IC-EMC.

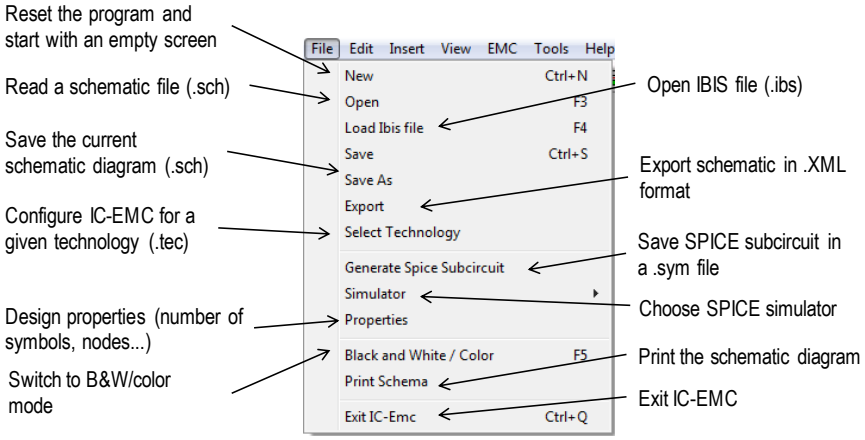


Figure 4- 1: The File menu

The Edit menu is used to create and change schematic diagrams.

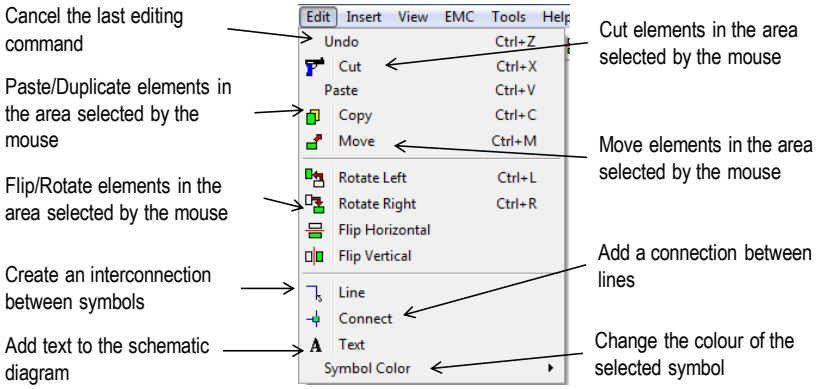


Figure 4- 2: The Edit menu

The Insert menu contains commands for inserting user or library symbols (.sym) that usually contain a user-defined SPICE subcircuit, other schematic diagrams (.sch), a component library (.lib), or SPICE analysis line.

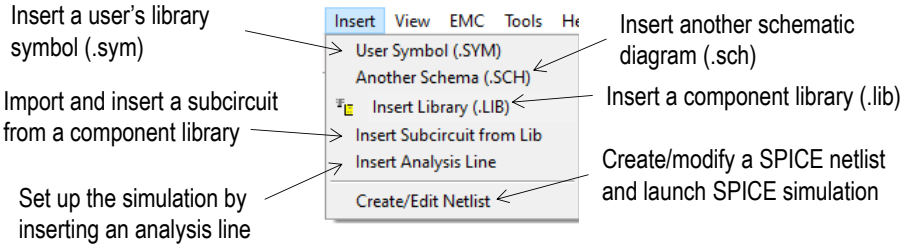


Figure 4- 3: The Insert menu

The View menu is used to zoom in or out of the schematic diagram. It also provides a tool for displaying electrical nets between components forming the schematic.

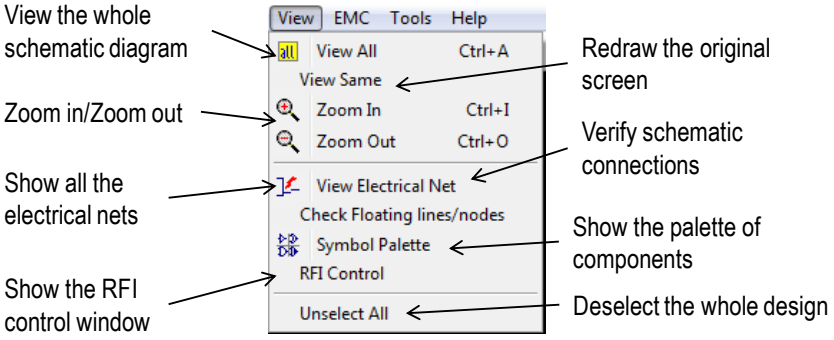


Figure 4- 4: The View menu

The EMC menu gives access to the main simulation and post-processing interfaces of IC-EMC, which are briefly summarised in part 3.3.

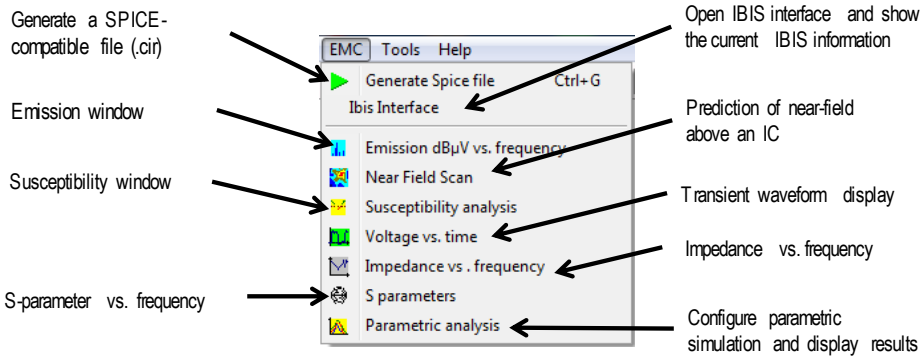


Figure 4- 5: The EMC menu

The Tools menu proposes various tools for generating models, building packages, PCB interconnects or cable models, analysing signals or performing conversions or simple evaluations useful for EMC (linear unit to dB, L-C resonant frequency, etc …).

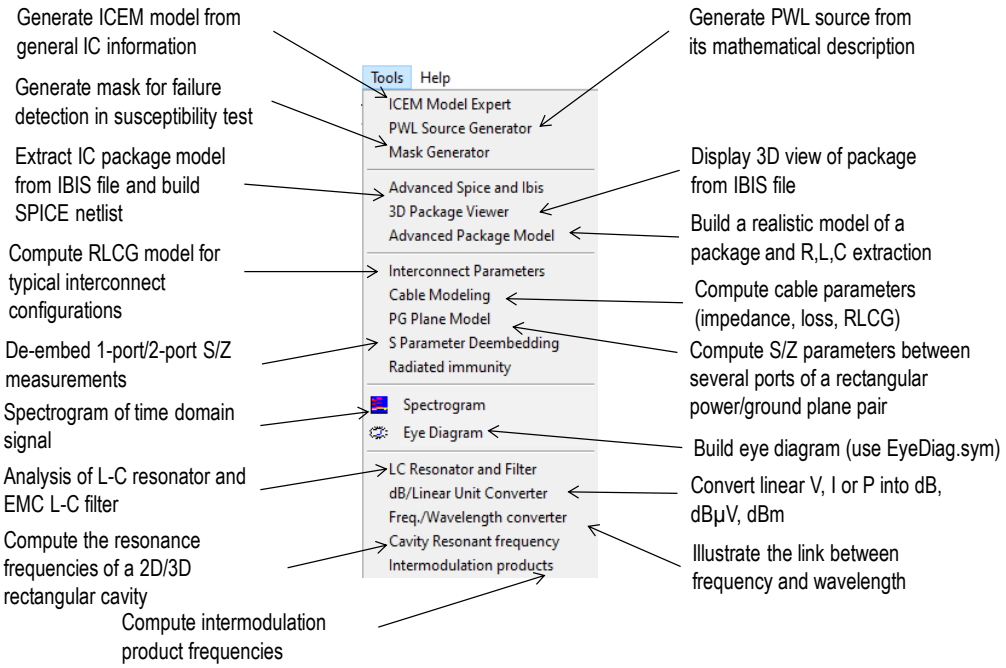


Figure 4- 6: The Tools menu

IV.2 Detailed commands of the menu File

IV.2.1 New (CTRL + N)

Click on “File > New” in order to restart the software with an empty screen. The current design should be saved before asserting this command, as all the graphic information will be physically removed from the computer memory. No Undo is available to disable the New command.

IV.2.2 Open (F3)

Click on the icon  . In the list, double-click on the file to load. " .SCH " is the default extension that corresponds to the schematic diagrams.

IV.2.3 Load Ibis File (F4)

Click on “File > Load Ibis File” lo load an IBIS file (extension .ibs) and open the IBIS interface. The IBIS interface can also be opened by clicking in the menu "EMC > IBIS Interface". See part III.5 for more details about the IBIS Interface.

IV.2.4 Save (CTRL+S), Save As

Click “File > Save” to save the schematic diagram with its current name. The default name is " EXAMPLE.SCH ". In the case of "Save As…", a new window appears, into which you are to enter the design name. Use the keyboard and type the desired file name. Press " Save ". Your design is now registered within the **.SCH** extension.

IV.2.5 Export

Extensible Markup Language (XML) has become a popular language to exchange data in a human and machine-readable format. Recently, XML format has been proposed for EMC purposes, such as exchange file for near-field measurement or simulation data [She09], and emission model [Ram15].

The command "File > Export" converts the schematic diagram displayed on the screen into a XML file. This schematic represents a model of an IC for conducted/radiated emission or immunity purpose. Figure 4- 7 shows the interface of this tool. The schematic examples\emission\mpc\mpc_vde.sch represents a simple conducted emission model of a 32 bit microcontroller (ICEM model). On the left part of the screen, the user can define the header of the file, that provides general information about the name of the model, its author, the name of the device, etc… and the purpose of the model in the part "Type of model". The components of model (R, L, C, sources) are also listed. On the right part of the screen, the content of the output XML file is displayed. The user can write in this part and change manually the content of the XML file. Clicking on the button Generate XML saves this content in the output XML file: several extensions are proposed for the file:

- .CEML: this XML file is dedicated for the exchange of conducted emission model
- .CIML: this XML file is dedicated for the exchange of conducted immunity model
- .XML: general purpose XML file

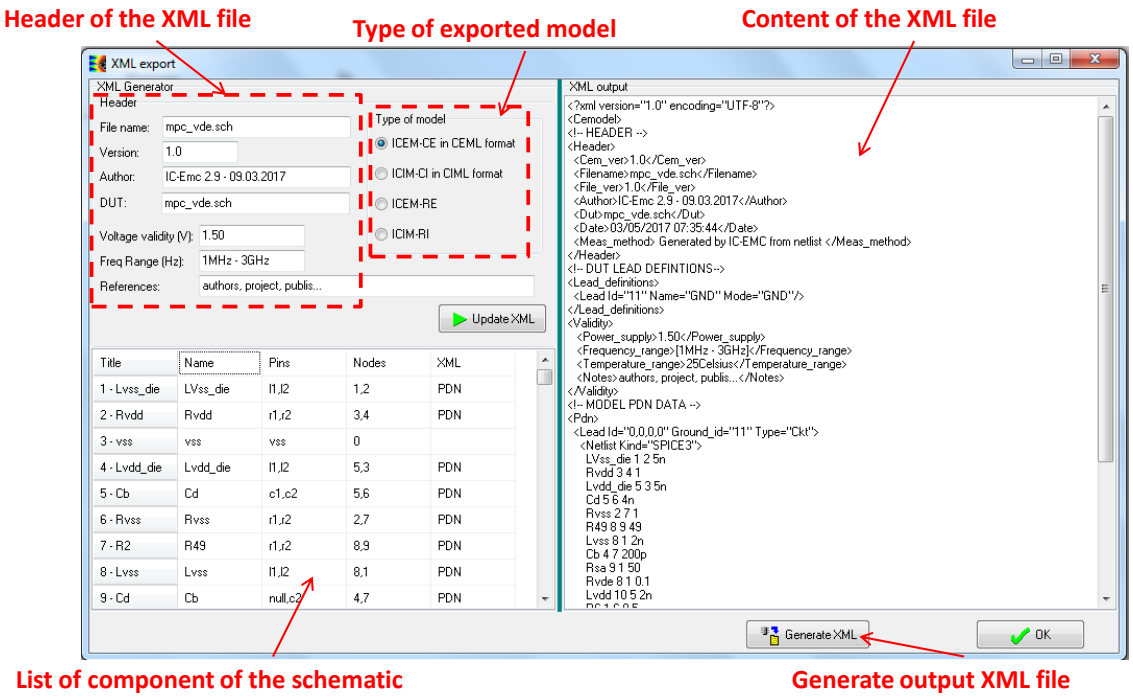


Figure 4- 7: Export of a schematic diagram in a XML file (examples\emission\mpc\mpc_vde.sch)

IV.2.6 Select Technology

Click on “File > Select Technology”. The list of available processes appears in .tec files. The initial design rule file is "default.tec". Various technologies are available from 1.2µm down to 22nm. Click on the rule file name and the software reconfigures itself in order to adapt to the new process. The .tec files are available in the directory "\lib". See Chapter VI for more information on the format of the TEC file.

IV.2.7 Generate SPICE sub-circuit

SPICE sub-circuit can be generated from a SPICE schematic containing subcircuit I/Os. Figure 4- 8 describes a schematic diagram with three I/Os placing at device terminals. Click on I/O and give and explicit name. These I/Os will be the external terminals of the SPICE subcircuit that we are going to generate.

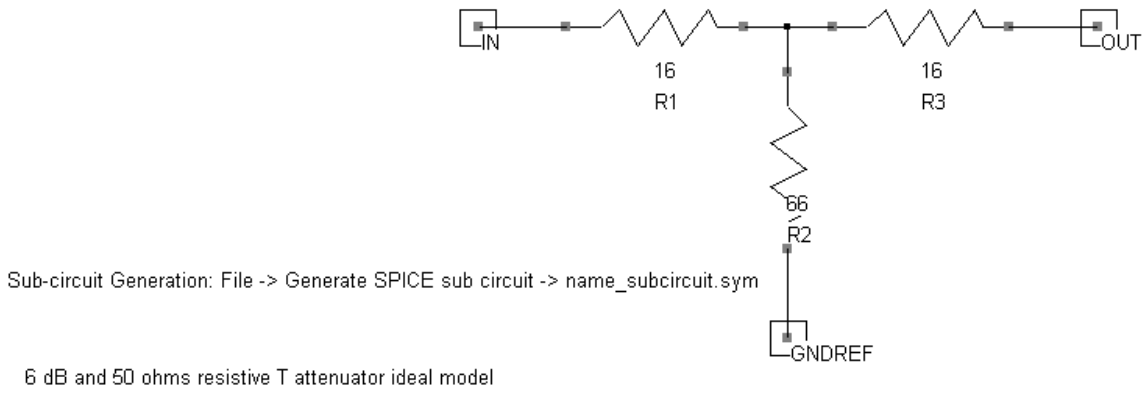


Figure 4- 8: Placement of subcircuit I/O on a schematic to generate a SPICE subcircuit (examples\EMC_lib\attenuator_6dB_subcircuit.sch)

Open the SPICE sub-circuit generation interface by clicking on **“**File > Generate Spice sub-circuit”. The following screen appears. The right part of the screen lists all the I/O of the device and their position (column “Side”), the left part describes the shape of the sub-circuit symbol. The position of I/O can be changed manually by modifying the property Side (‘L’, ‘R’, ‘T’ or ‘B’ for Left, Right, Top and Bottom respectively) and clicking on the button Refresh. The size of the subcircuit symbol can be updated with the buttons  . The subcircuit SPICE description and the graphical symbol are saved in a *.sym file. By default, the name of the *.sym is identical to the schematic name. Change the field “Name” and Save as:” to modify the names of the *.sym file and the SPICE sub-circuit. Click “OK” to generate the *.sym file. Click **“**Insert > User symbol” to add the symbol of the subcircuit in a schematic. If you click on the subcircuit symbol, the SPICE description of the subcircuit is edited.

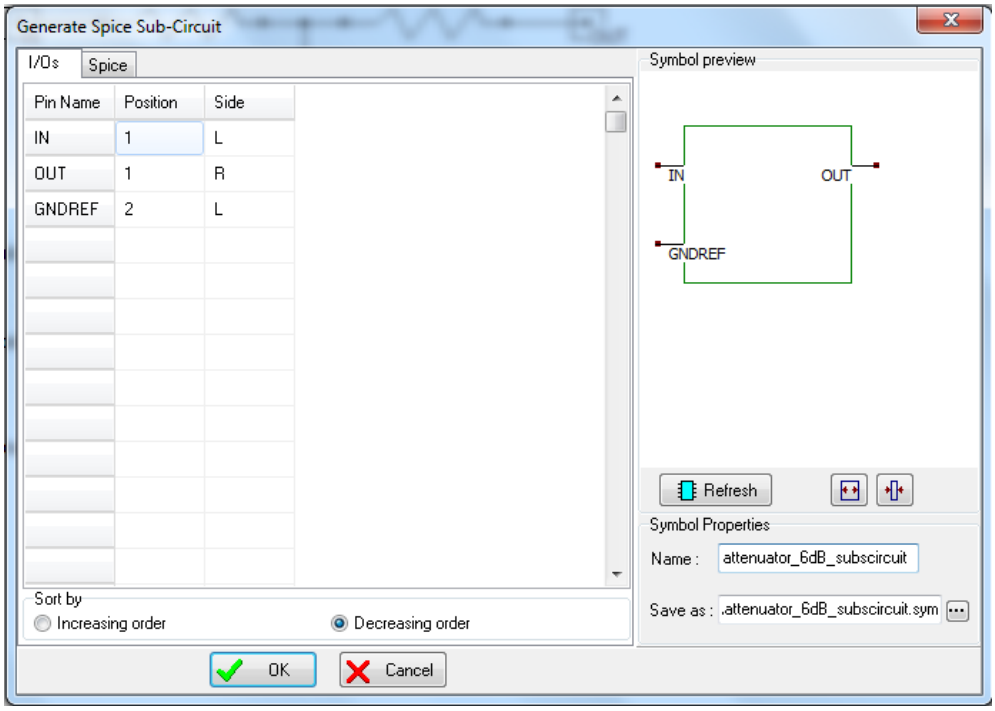
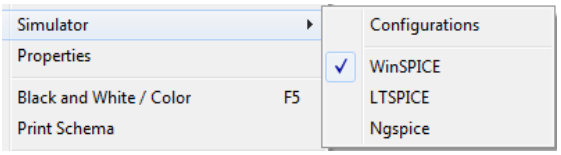


*Figure 4- 9: Generating a SPICE sub-circuit and the graphical symbol, saved in a *.sym file (EMC_lib\attenuator_6dB_subcircuit.sym)*

IV.2.8 Simulator

The menu "File > Simulator" gives access to several options to select the SPICE simulator (WinSPICE, LTSPICE or Ngspice) and configure the simulation.



Click on "WinSPICE", "LTSPICE" or "Ngspice" menu to select the SPICE simulator. Clicking on "Configurations" menu opens the following screen. In the upper part of the screen, the path of the WinSPICE, LTSPICE and Ngspice simulators have to be defined (executable files wspice3.exe for WinSPICE, scad.exe or XVIIx64 for LTSPICE, ngspiuce.exe for Ngspice). This operation has to be done manually each time the user reinstalls SPICE simulators and their installation directories. In the lower part of the screen, three simulation options are proposed:

- Launch simulator manually: when the user generates SPICE netlist , he has to launch the simulator, opens the circuit netlist (.cir file) and launch the simulation
- Interactive mode: when the user generates SPICE netlist , the simulator is automatically launched and remains opened at the end of the simulation to analyze the result
- Batch mode: when the user generates SPICE netlist , the simulator is automatically launched but is closed directly at the end of the simulation

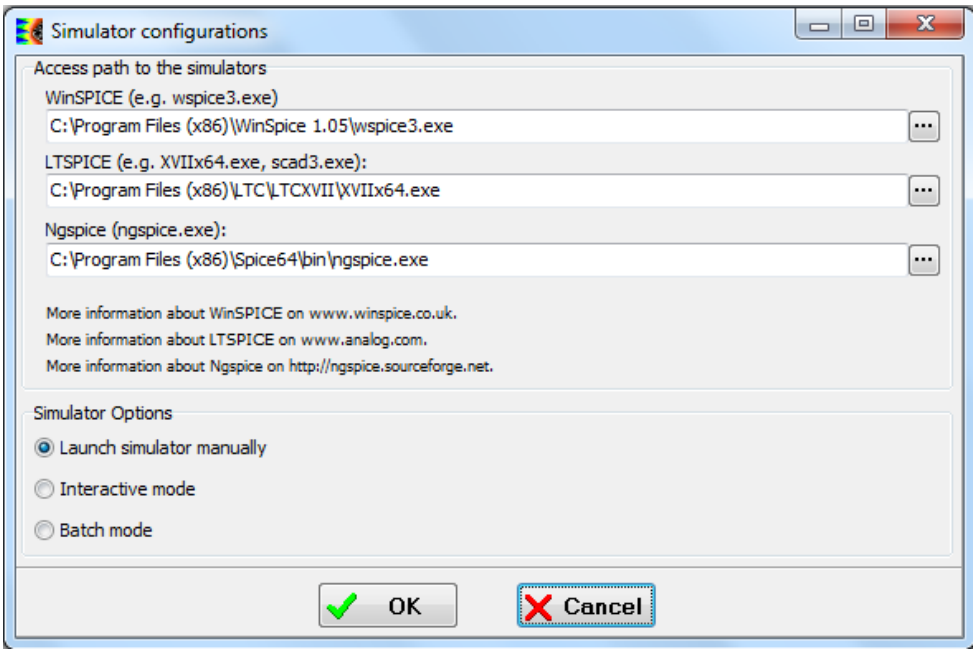


Figure 4- 10: Simulator configurations

IV.2.9 Properties

The command “File > Properties” provides some information about the current technology, the percentage of memory used by the schematic diagram and its detailed contents (Figure 4- 11). It gives also an access to some special options for schematic design and debug features.

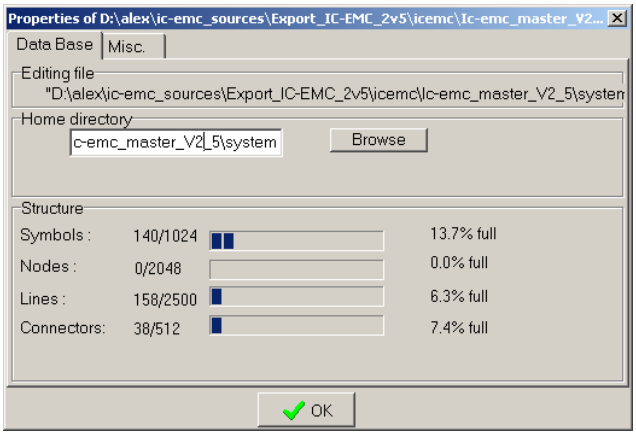


Figure 4- 11: File properties, including statistics about the number of symbols, nodes and lines

IV.2.10 Black and White /Color (F5)

The command “File > Black and White/Color” switches to black and white display mode: the layout is drawn in black and white. This type of drawing is convenient to build black and white documentation by avoiding a black background. Alternatively, press “Alt”+”Print Screen” to copy the active window to the clipboard. Then, open Microsoft Word™ or WordPad, click “Edit > Paste”. The screen is inserted into the document.

IV.2.11 Print Schema

Click on "File > Print Schema" to transfer the graphical contents of the screen to the printer. Alternatively, you can make a copy of the window into the clipboard in order to import the screen into your favorite text editor by pressing <Alt>+<Print Screen>. In the text editor or in the graphic editor, simply click on “Edit > Paste” We recommend that you switch to monochrome mode first by invoking the function "File > Black and White / color". In that case the layout will be drawn in a white background color using gray levels and patterns.

IV.2.12 Exit IC-EMC (CTRL+Q)

Click on "File > Exit IC-EMC" (or CTRL+Q) in the main menu. If you have made a design or if you have modified some data, you will be asked to save it. After confirmation, you can return to Windows.

IV.3 Detailed commands of Menu Edit

IV.3.1 Undo (CTRL+Z)

The Undo command (“Edit > Undo”) is useful to cancel the last editing command. It is possible to undo the commands Cut, Paste, Copy, Move, Stretch and Edit.

IV.3.2 Cut (CTRL+X)

Click on the Cut icon  or on “Edit > Cut”. Move the cursor to the design window, and delimit the active area with the mouse. Consequently, all the graphics included in this area are erased. Click on Undo to fix those elements back into the design. One symbol only can be erased by a click inside its shape when the cut command is active. The symbol is then erased. One single interconnect can be erased by a click on its wire when the cut command is active.

IV.3.3 Paste (CTRL+V)

Invoke the *Paste* command “Edit> Paste”. All previously copied elements are pasted at the desired location. Deleted elements can be replaced that way. Click “**Undo”** to cancel the *paste* command.

IV.3.4 Copy (CTRL+C)

Click on the Copy icon  , or on “Edit > Copy”. Move the cursor to the design window, and delimit the active area with the mouse. Consequently, all the graphics included in this area are copied. The external shape of the copied elements appears. Fix those copied elements at the desired location by a click on the mouse. Click on Undo to cancel the copy command.

IV.3.5 Move (CTRL+M)

To move one graphical element, click on the "Move" icon  or **"**Edit > Move". Then using the mouse, draw an area that includes the elements. Then, drag the mouse to the new location and release the mouse. As a result, the elements are moved the new place. One single line can be moved or stretched (depending where you click) by a direct click on the line. One single text can be moved by a direct click on the text location.

IV.3.6 Rotate (CTRL+R or CTRL+L)

To apply a rotation to one part of the design, click “Edit > Rotate”. Select one of the proposed action:

- Rotate right or 90° 
- Rotate left or -90° 

Then, delimit the area inside which the elements will be rotated. To rotate one single symbol, simply place the cursor above the desired symbol and press CTRL+R.

IV.3.7 Flip Vertical/Horizontal

To apply a horizontal or vertical flip to one part of the design, click on icons  or  , or “Edit > Flip”. Then, delimit the area inside which the elements will be changed.

IV.3.8 Line

The " Line " icon  is activated by default. It creates an interconnection between two points in the schematic diagram. If the " Line " icon is not selected, click on it. Another method to select it consists in a right click with the mouse. Then, move the cursor to the display window and fix the start point of the interconnect with a press of the mouse. Keep pressed and drag the mouse to the interconnect end. Release the mouse and see how the line is created.

IV.3.9 Connect

Use the icon  command “Edit > Connect” command to create the electrical contact between crossing interconnects. Contacts are normally created automatically when the Line icon is selected and a click is made above an existing interconnect to create a second interconnect.

IV.3.10 Text

Use this icon  or "Edit > Text" to define a text to one box or location in the design. That text sets simulation commands, illustrates the layout and should be used as much as possible for each significant node such as inputs and outputs. To add some text to a particular place, proceed as follows:

1. Click on the icon
2. Set the text location with the mouse. A dialog box appears
3. Enter the text in front of “Text:” and press “Ok”. The text is set in the drawing

A text can be modified as follows: click on the icon, click inside the existing text. The old text appears. Modify it and click on “Ok”. Text is added for information only. It has no impact on simulation.

If text is added for information only, it has no impact on simulation. Text is useful to add comments on the schematic diagram, add more information or specific I/Os or nodes.

Note that text starting with “.” is usually considered as a simulation command. For example: “.TRAN 0.1NS 100NS” is a text that is also considered as a SPICE control to configure the transient simulation. The table below lists the main SPICE simulation commands that can be inserted in schematic diagram. Some of these commands can be automatically placed through the menu "Insert > Insert Analysis Line".

Keyword	Used for	Example	Parameters
.TRAN	transient simulation	.TRAN 0.1NS 100NS	Step, duration
.DC	dc simulation	.DC Vin 0 5 0.1	Voltage, start voltage, stop voltage, voltage step
.AC	AC simulation	.AC DEC 10 1MEG 1G	DEC = decade, points per decade (10), start freq (1 MHz), stop freq (1 GHz)
.IBIS	Load IBIS file	.ibis cesame_v14.ibs	Name of the Ibis file
.LIB	Load SPICE library	.lib cesame.lib	Name of the text file that includes the component models. The default library is ‘spice.lib’
KA	Inductance coupling	K2 Ltem2 Lvdd 0.002	Coupling between inductor 1, inductor 2 and coupling coefficient (between 0 and 1)
.OPT	WinSpice option	.OPT RELTOL=1e-6	.OPT RELTOL=1e-6
.SCAN	Scan configuration	.scan 1e-3 10e6 3.5e-3 2.1e-3	Scan step (1e-3), scan frequency (10 MHz), scan altitude (3.5 mm) and lead

			altitude (2.1 mm)
.PLOT	Plotting signals	.plot v(1) .plot –i(vsource)	Lists the voltage or current to appear in the Spice simulation
.FAIL	Immunity threshold	.fail 1.0V .fail < 0.5V	Fixes the voltage threshold used in immunity simulation. The signs '>' or '<' indicate a rise or fall edge detection.
.VDD	Supply Voltage	.vdd 3.3V	Fixes the general supply voltage to the desired value. Otherwise, the default VDD value of the technology file (default.tec) is used.
.SCRIPT	Add a script from a text file	.script iteration.txt	Replace the 'run' section in the Spice netlist by the text contained in the user's defined text.
.TEMP	Define temperature	.temp 85	Defines the simulation temperature. By default, 25°C is used.

Table 4- 1: Main SPICE simulation commands which can be inserted as text in schematic diagram

IV.3.11 Symbol Color

The command "Edit > Symbol Color" is useful to change the color of a group of symbols included in a given area. The same result is obtained by successively clicking inside each symbol and altering the color parameter. It is recommended to assign different colors to different parts of the schematic diagram.

A proposed color assignment is as follows:

- IC-related symbols are in yellow
- Package-related symbols are in red
- Probe-related symbols are in blue
- External symbols are in green (default color)

IV.4 Detailed commands of Menu Insert

IV.4.1 Insert User Symbol (.SYM)

The command "Insert > User Symbol" is used to add a user defined symbol to the existing schematic diagram. A user symbol can be created using the command "File > Schema To new Symbol". The inserted symbol can be fixed at the desired location.

IV.4.2 Insert another Schema (.SCH)

The command "Insert > Another Schema (.SCH)" is used to add a schematic diagram .SCH file to the current schematic diagram. Its content is fixed at the right lower side of the current schematic diagram. The current file name remains unchanged.

IV.4.3 Insert Lib .LIB)

The command “Insert > Insert Lib” allows the selection of a *.lib file through a Windows explorer windows (Figure 4- 12). *.LIB files contain library of device models and parameters (diodes, transistors, transmission lines…). It is necessary to include the library path name and file name in an IC-EMC schematic which include a component with a model declared in a library file.

Another method to include a library in an IC-EMC schematic consists in writing on the schematic a text line (with the command “Edit > Text”) such as “.lib path_name\file_name.lib”

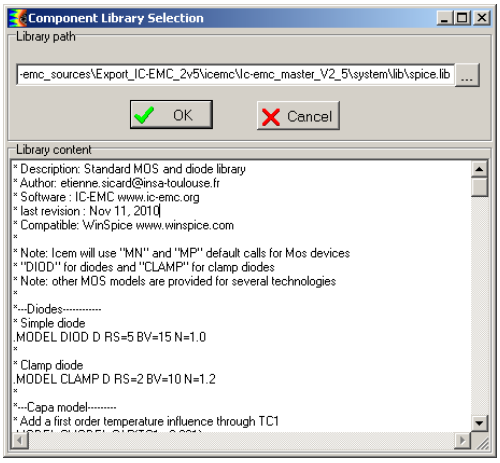


Figure 4- 12: Selection of a library file (.lib)*

A default library is provided in ‘lib\spice.lib’. Any library file can be imported, only if it is compatible with WinSPICE, LTSPICE or Ngspice syntax (refer to the documentation of solvers).

The following extensions are supported:

- .lib
- .mod
- .mos (library of MOSFET model from LTSPICE)
- .dio (library of diode model from LTSPICE)
- .bjt (library of bipolar junction transistor model from LTSPICE)

IV.4.4 Insert Subcircuit From Lib

Manufacturers of electronic components (especially passive devices) often provide models of components as SPICE subcircuits (.subckt) within a library, usually a non-crypted ASCII file. With this menu, the component library can be imported and the different component model can be visualized. One component of the imported library can either be directly inserted in the electrical schematic or saved within a user symbol (.sym). The symbol can be placed later in the schematic, according to the approach described in I.4.1.

The following file extensions are supported. They are related to the component library of several well-known passive device manufacturers (Wurth Elektronik, Murata, Panasonic, TDK (EPCOS), KEMET (Yageo) :

- .lib
- .mod
- .sub
- .ckt

The figure below shows the interface. Select the library file and click on the button Read to import the library file. The content of the library is edited on the left part of the screen. The different subcircuits found in the library file are listed in the list “Select Subcircuit”. For each subscircuit, the number of terminals are given in the field “Number of I/O pads”.

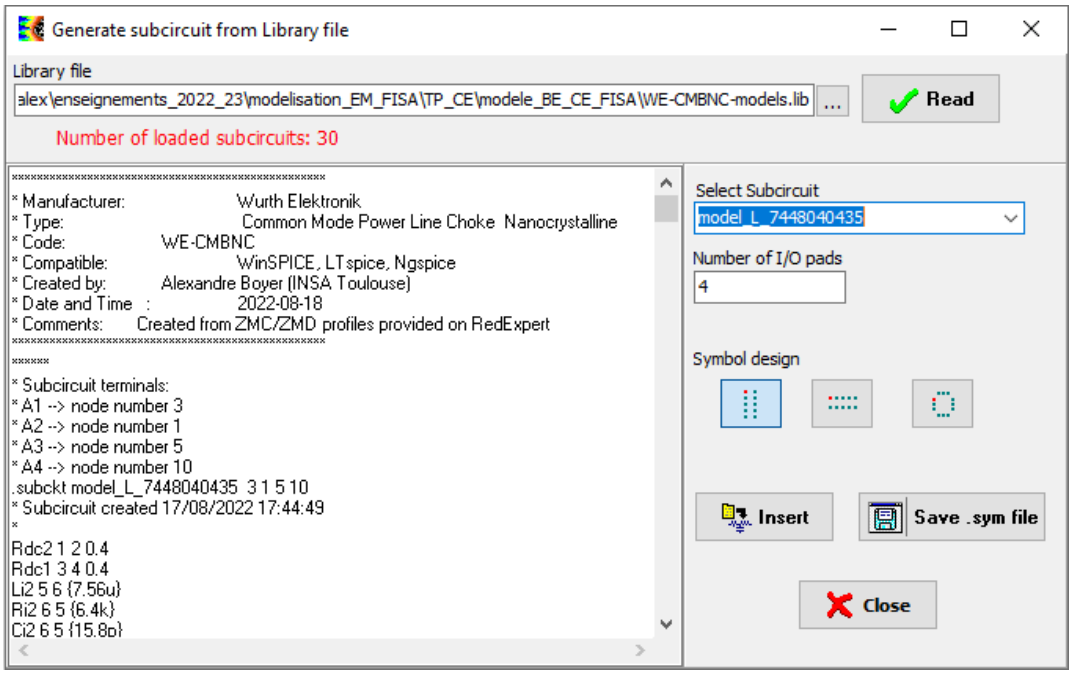


Figure 4- 13: Import of a library of component models (SPICE subcircuit) and insertion on schematic

One subcircuit can be selected in the list “Select Subcircuit” and placed on the schematic according to two different methods:

1. If you click on the button “Insert”, the selected subcircuit can be placed directly on the schematic. Click on the button “Close” to close the interface. The subcircuit symbol can be placed anywhere on schematic, depending on where you click.

2. If you click on the button “Save .sym file”, the selected subcircuit (its graphical symbol and the SPICE netlist) will be saved in symbol file (.sym) for future use. The user symbol will be placed later with the command “Insert > User symbol (.SYM), as explained in I.4.1.

Whatever the placement method, the design of the graphical symbol can be selected according to one the three configurations given by the buttons “Symbol design”. The graphical symbol is a rectangular shape. The positions of the I/O terminals are either along the left/right sides, top/bottom sides, or the four sides of the graphical symbol.

IV.4.5 Insert Analysis Line

Click on “Insert > Insert analysis line” to place automatically a simulation command line on the schematic diagram. An interface dedicated to the configuration of the SPICE simulation is opened and the analysis line is automatically inserted on the schematic with the correct syntax. Figure 4- 14 shows the interface, which presents several tabs. One tab is dedicated for one type of command:

- DC analysis: to configure .DC sweep analysis
- AC analysis: to configure .AC small signal analysis
- Transient analysis: to configure transient analysis
- Temperature sweep: to configure sweep of ambient temperature
- SPICE options: to configure the different options of the SPICE simulators (refer to your SPICE simulator documentation for more information about these options)
- Near-field scan options: to set the options of near-field simulation (refer to part III.8)

Each tab proposes boxes and fields to configure the different options. On the lower part of the screen, the command line that will be added on the schematic diagram is displayed and updated when options are changed. This command line can also be directly typed. A verification of the syntax is performed. Click on the button Insert to place automatically the command line on the schematic diagram.

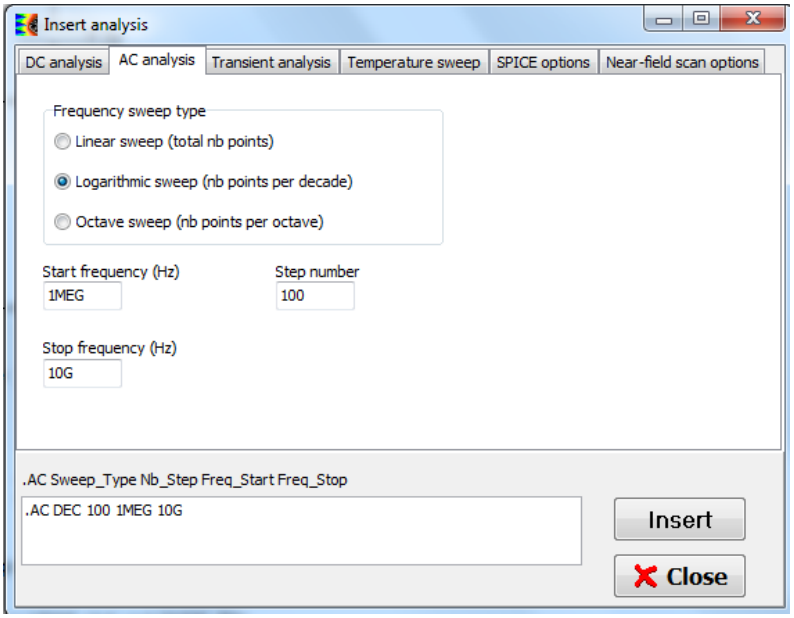


Figure 4- 14: Insert a simulation command line on the schematic ("Insert > Insert analysis line")

IV.4.6 Insert Netlist

Click on "Insert > Insert Netlist" to place SPICE components into the schematic diagram from a netlist description. Figure 4- 15 presents the interface and the different steps.

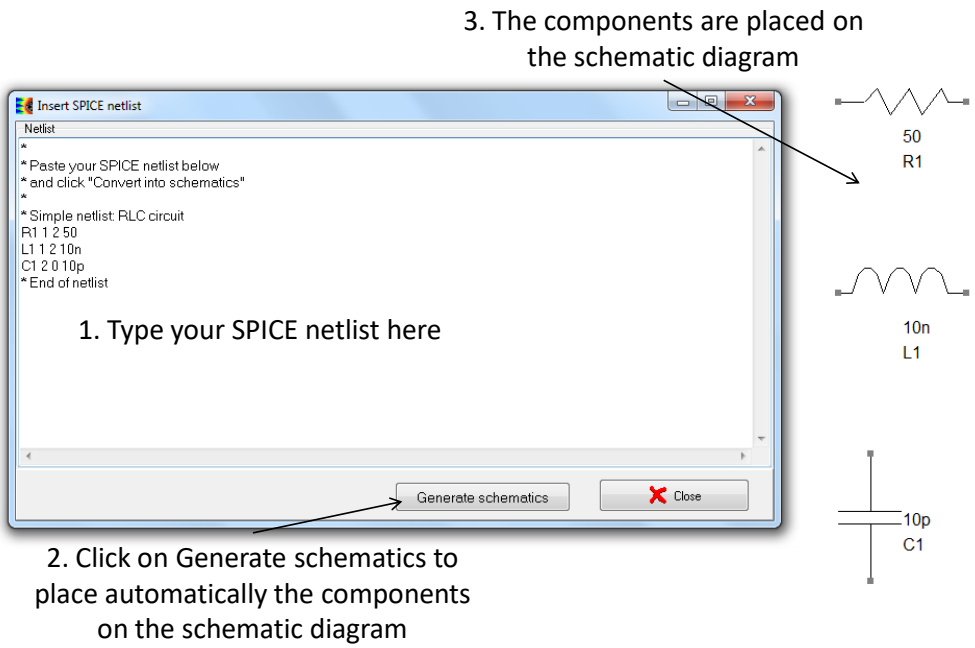


Figure 4- 15:Type a SPICE netlist and insert the components on the schematic diagram ("Insert > Insert Netlist")

IV.5 Detailed commands of Menu View

IV.5.1 View All (CTRL+A)

Click “View > View All” or on the icon  to fit the screen with all the graphical elements currently displayed on the screen.

IV.5.2 View Same

Click “View > View same” to draw again the schematic diagram without changing the scale. This function is used to refresh the screen.

IV.5.3 Zoom In & Out (CTRL+I and CTRL+O)

The icons  and  perform Zoom In and Zoom Out. these commands are also available in the menu "View > Zoom In" and "View > Zoom Out". When zooming in, the area determined by the mouse will be enlarged to fit the display window. When zooming out, the area determined by the mouse will contain the display window.

- If you click once, a zoom is performed at the desired location.
- Press Ctrl+A for « View All », and Ctrl+O for zoom out.

IV.5.4 View Electrical Net

Click on the icon  or on “View > View Electrical Net”. Then, click in the desired interconnect or pin in the schematic diagram. After an extraction procedure has been carried out, you will see that all the wires connected to that node. Click <Escape> or “View > Unselect All” to unselect the diagram.

IV.5.5 Check Floating Lines / Nodes

The command "View > Check Floating Lines / Nodes" can detect problems of interconnections in the schematic. The schematic diagram is scanned in order to detect interconnects with a wrong connection to the symbol or other interconnects, as in Figure 4- 16.

The tool “Check Floating Lines” is launched automatically each time the button “Generate SPICE File” is clicked before the generation of the SPICE netlist.

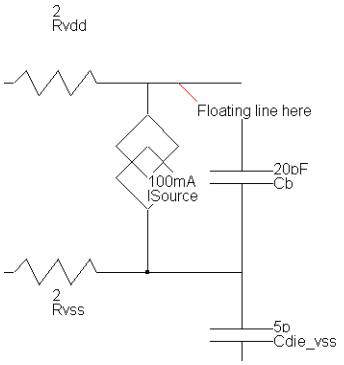


Figure 4- 16: Example of floating line

IV.5.6 Symbol Library

The palette symbol library contains basic electrical symbols, sources, probes and switches. The palette is visible by default. It can be closed by the user. The command "View > Symbol library" or the icon  makes the palette visible. The symbol library is reported in the reference manual. Additional symbols may be found in the “ieee” sub- directory, accessible through the command "Insert > User Symbol". Refer to chapter V for the list of symbols available in the palette.

IV.5.7 RFI control

The command "View > RFI Control" is used to open the susceptibility simulation configuration interface (see part III.4 for an example of susceptibility simulation). This simulation requires the presence of a RFI source and a coupler in the IC-EMC schematic.

IV.5.8 Unselect All (Escape Key)

Use the command “View > Unselect All” to cancel undesired commands, or to redraw the complete schematic diagram.

IV.6 Detailed commands of Menu EMC

IV.6.1 Generate SPICE File (CTRL+G)

IC-EMC converts the SCH schematic diagram into Spice format using a specific interface (**Erreur ! Source du renvoi introuvable.**), invoked by "EMC → Generate SPICE file" or by the icon  . The SPICE file can be exported to analog SPICE-compatible simulators such as WinSPICE and LTSPICE.

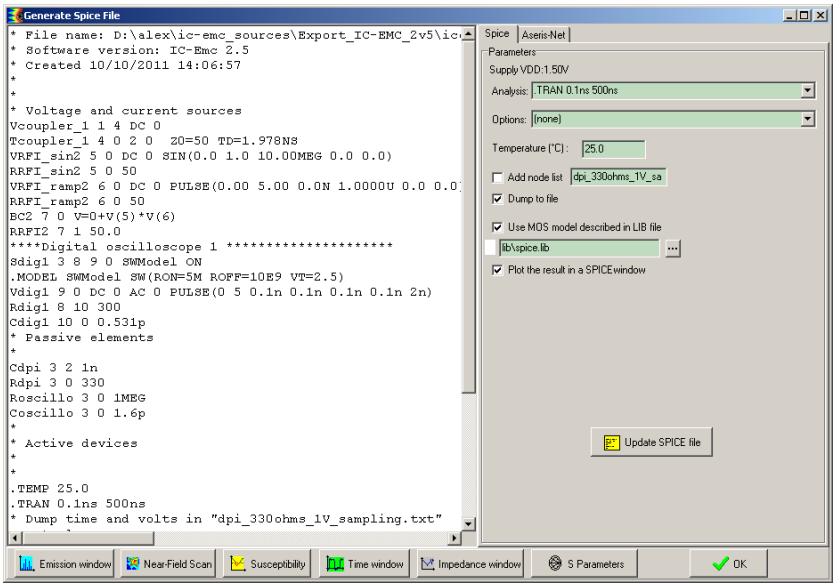


Figure 4- 17: Converting a schematic diagram into a SPICE-compatible text file

IV.6.2 Ibis Interface

The IBIS interface is opened by the command "EMC > Ibis Interface" or with the icon  . It enables the presentation of IBIS data file (Figure 4- 18), and to control a set of commands related to the exploitation of the IBIS information. An example of utilization of the IBIS interface is given in part III.5. The IBIS file is edited in read-only mode in the left part of the screen. Several tab windows are available in the right part of the interface:

- I/O: the list of the I/Os, the associated models and R, L, C stray elements given by IBIS file are summarized.
- Models: parameters of the I/O models are listed and their characteristics can be plotted (see III.5.2).
- Infos: general information about the IBIS file (version, date, manufacturer, etc), conditions and package are given
- Package: a 2D view of the package is reconstructed by IC-EMC from the pin list and keywords added by the user (see III.5.3).:

Several control buttons are available in the lower part of the IBIS interface. The button "**3D Draw**" open a window showing the package in 3D with a user control of the 3D view. This window can also be opened with the command "Tools > 3D package viewer". the button

"**Advanced SPICE and IBIS**" gives access to an interface to evaluate stray RLC elements of package, build SPICE compatible model and resource IBIS file.

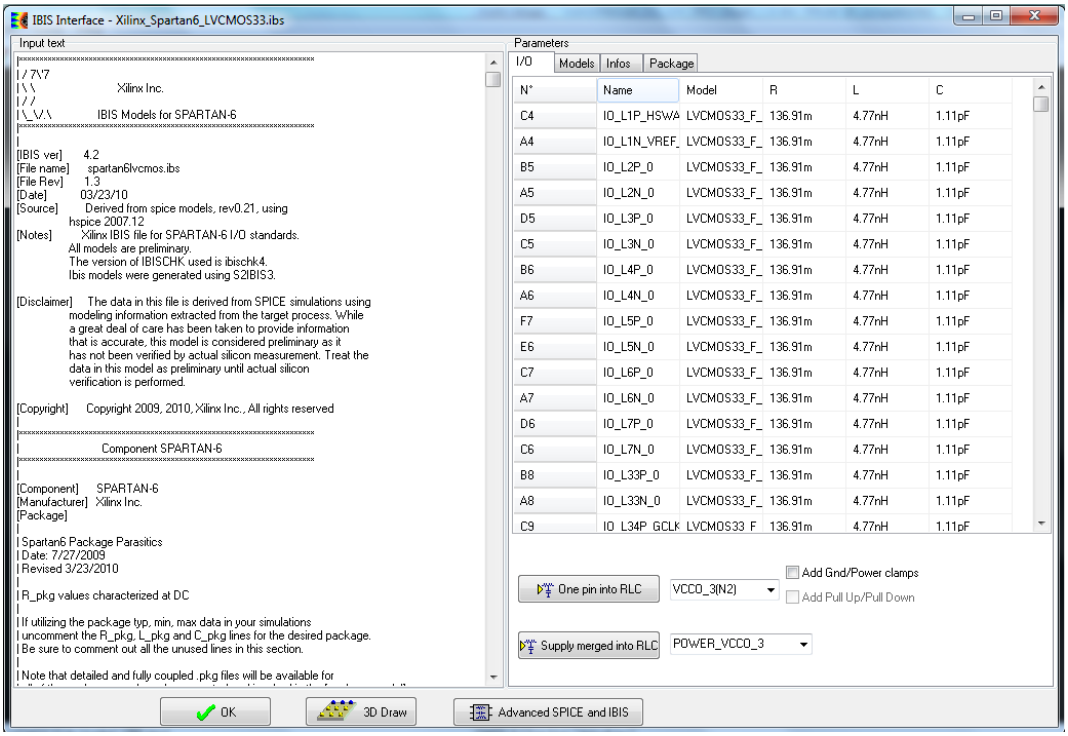
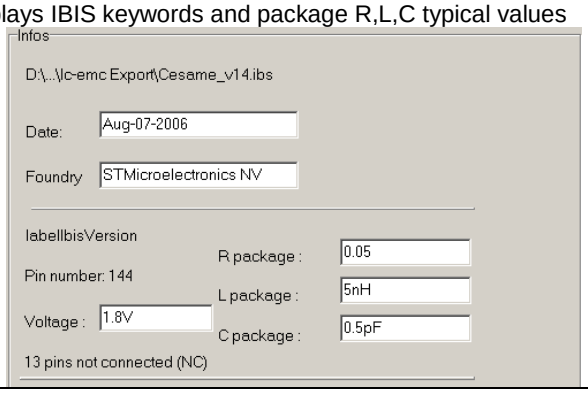


Figure 4- 18: The IBIS interface

The other sub-commands are listed below.

Sub Menu	Command	Description
"I/Os"	One Pin Into R,L,C	Choose the desired pin that will be converted into a R,L,C circuit according to the information available in the R_pack, L_pack, C_pack variables of the [Package] sub-section.
	Supply Merged into R,L,C	Choose the desired supply model. All pins with the associated model will be converted into a R,L,C circuit according to the information available in the R_pack, L_pack, C_pack variables of the [Package] sub-section. The resistance will be divided by the number of pins, as well as the inductance. The capacitance will be multiplied by the number of pins.

Sub Menu	Command	Description
"Models"	Y axis	Change the Y scale
	From A, to A	Manually define the Y axis boundaries
	Draw	Redraw the I/V current
	Dump	Save the I/V curve in a ibis-compatible format
	PU	Draw pull-up I/V information if available
	PD	Draw pull-down I/V information if available
	Pc	Draw Power-clamp I/V information if available
	Gc	Draw Gnd-clamp I/V information if available
	RW	Draw rising-waveform V(t) if available
	FW	Draw falling-waveform V(t) if available
	Add Data	Add a simulated I/V or V/t from a Spice simulation to compare with the current I/V or V/t from IBIS. The "TXT" format assumes 3 columns (index, voltage, current), the "DAT" format assumes 2 columns (voltage, current).
	-Sign	Changes the sign of the loaded data through command "Add Data"

Sub Menu	Command	Description
“Info	None	Displays IBIS keywords and package R,L,C typical values 

Sub Menu	Command	Description
Package	I/O color	Changes the I/O color in the 2D-view of the package
	Background Color	Changes the I/O color in the 2D-view of the package
	Display coordinates	Adds the [x,y] numbers or letters to the 2D-view
	Display names	Add all package pin names to the 2D-view
	Locate Pin	Select the desired pin which will appear in purple in the drawing, with an estimation of the 2D-position
	View	Top view or rear view. By default, top view.

IV.6.2.1 Hidden Physical Information

Some important information is resourced in the IBIS file related to the package and IC physical dimensions. The information is placed in the [Package model] section, and starts by « | » to avoid parsing errors with conventional IBIS loaders. The physical dimensions are very important information to rebuild the lead frame structure of the package, together with the bonding structure and access to the die.

Hidden parameter	Description	Example
pack_width	Package width	20.1e-3 m
pack_height	Package height	20.1e-3 m
ic_width	Die witdh	6.55e-3 m
Ic_height	Die height	6.33e-3 m
ic_xstart	Die location in X related to the package	6.73e-3 m
ic_ystart	Die location in Y related to the package	6.84e-3 m
ic_thick	IC thickness	500e-6
pack_pitch	Package pin pitch	0.5e-3 m
Lead_alt	Lead altitude over ground plane	0.5e-3 m
ic_altitude	Die altitude over the ground plane	0.8e-3 m
Pack_ball	BGA ball radius	0.25e-6 m

Table 4- 2: Hidden parameters stored in the [package model] section

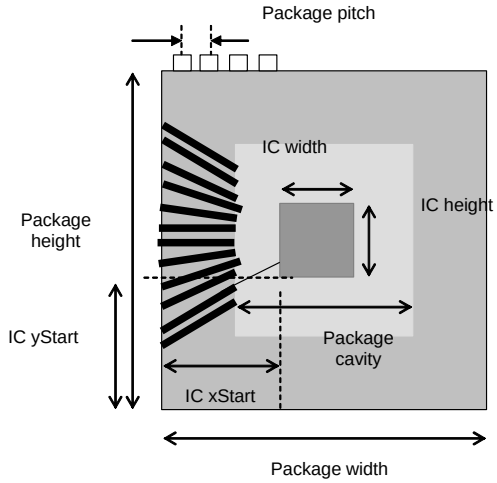


Figure 4- 19: Top view of the package

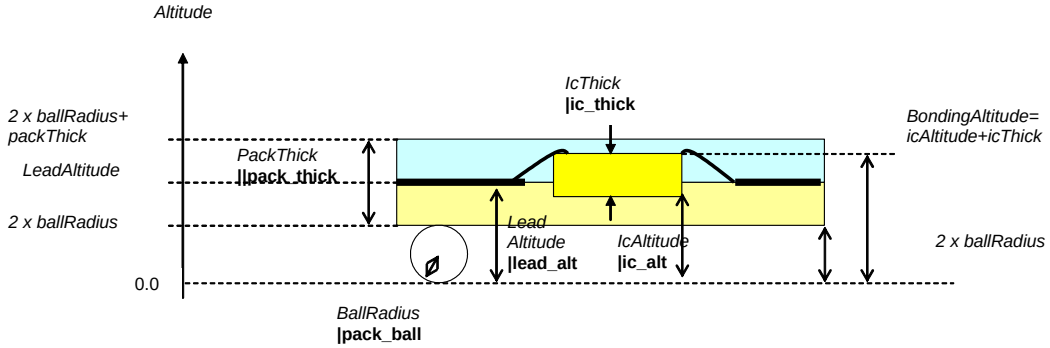


Figure 4- 20: Cross-section and main physical parameters describing a package

IV.6.3 Emission vs. frequency

The command "EMC > Emission vs. Frequency" opens a screen dedicated to the plot of spectrum of simulated and measured transient signals. Measured spectrum can also be loaded for direct comparison with simulation. The voltage waveform computed by the analogue simulator is translated into the frequency domain according to two methods:

- FFT mode: by default with a Fast Fourier Transform (FFT)
- EMI receiver mode: the effect of the intermediate frequency (IF) filter of an EMI receiver followed by a peak detector is simulated. This simulation is also based on a FFT. More explanation about the principle of the simulation can be found in the following reference: C. Li, L. Zhang, T. Dong, T. Wong, H. Chen, " An EMI Receiver Model with Consideration of the Intermediate Frequency Filter", 7th Asia-Pacific Int. Symp. on EMC, May 2016.

The default screen when a simulation result is loaded is described in Figure 4- 21. The emission spectrum is the Fourier Transform of the time-domain SPICE simulation stored in the file given in the field “Simulation file” in the tab "Input data". The X and Y axis and curve appearance may be modified using the commands available in the tab "Display". The FFT parameters may be modified with the tab "FFT" (number of points, window type, initial time) may be adjusted manually.

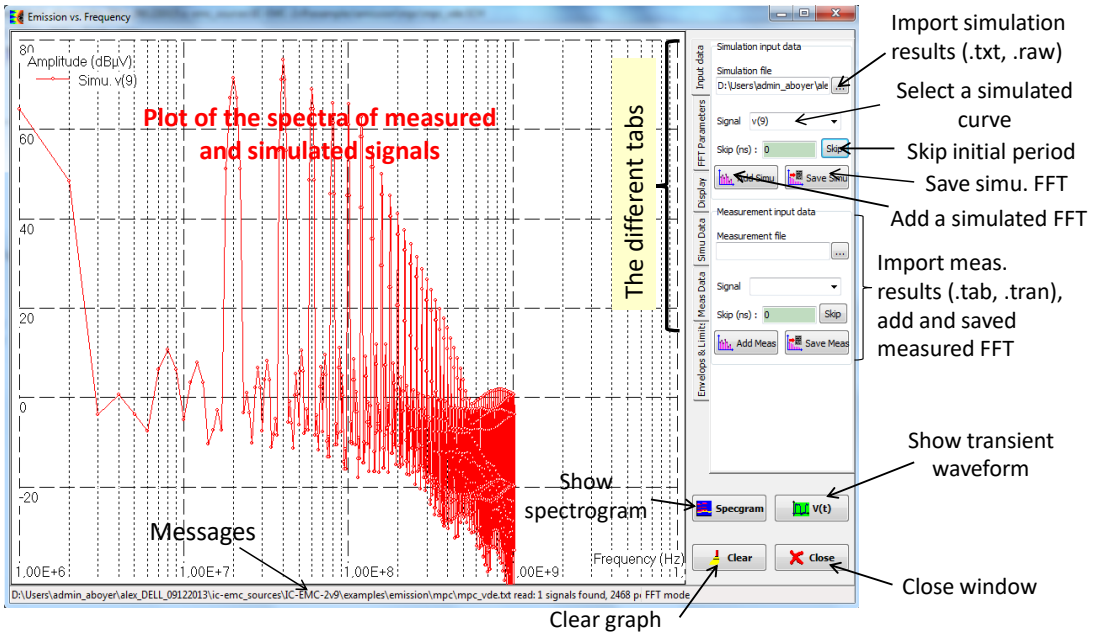


Figure 4- 21: the window "Emission vs. Frequency"

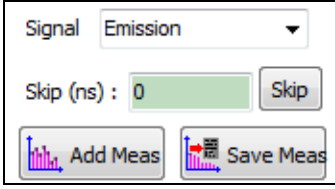
Different buttons appear on the bottom right of the window:

- V(t): shift to time-domain mode
- Specgram: shift to spectrogram mode
- Clear: remove simulated and measured spectra
- Close: close the window and returns to the main screen

IV.6.3.1 Tab "Input Data"

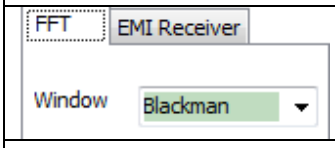
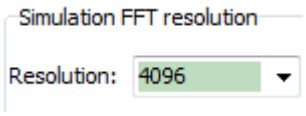
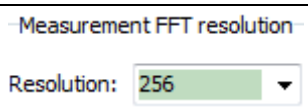
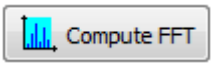
In this tab, the input simulation and measurement result file can be imported.

Buttons	Description
Simulation input data Simulation file s\basic\Voltage_Divider.txt …	Import simulation transient results from WinSPICE (.txt file) or LTSPICE (.raw file). Click on the button … to select the file.
Signal v(1) Skip (ns) : 0 Skip Add Simu Save Simu	Select the simulated transient signal to be displayed in the list "Signal" and click on the button "Add Simu" to plot its spectrum. The initial period of the transient signal can be skipped. Click on the button "Save Simu" to save the simulated spectra in a .tab file.
Measurement input data Measurement file mples\basic\s12x_tem.TAB …	Import measurement results either in time-domain (.tran file) or in frequency domain (.tab file). Click on the button … to select the file. In case of import of a .tran file, the spectrum of the imported signals is computed by FFT.

	Select the measured signal to be displayed in the list "Signal" and click on the button "Add Meas" to plot its spectrum. In case of the import of a.transient signal, its initial period can be skipped. Click on the button "Save Meas" to save the measured spectra in a .tab file.

IV.6.3.2 Tab "FFT Parameters" - FFT mode

Select the tab "FFT" to choose the FFT mode.

Buttons	Description
	Select the windowing options to compute the FFT of simulated and measured signals. Three types of window are proposed: Blackman (by default), Hamming and rectangular.
	Set the resolution or the number points of the FFT of the simulation results in the list "Resolution". The proposed values are power of two and range between 128 (the minimum resolution) and the best resolution with the on-going simulated signal. This term is related to the number of points of the imported transient signal. The maximum resolution is limited to 262144.
	Set the resolution or the number points of the FFT of the measurement results (.tran file) in the list "Resolution". This list is visible only if a .tran signal has been imported. The proposed values are power of two and range between 128 (the minimum resolution) and the best resolution with the on-going measured signal. This term is related to the number of points of the imported transient signal. The maximum resolution is limited to 262144.
	Update FFT of the plotted simulated and measured signals.

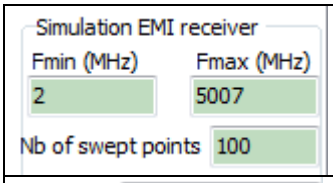
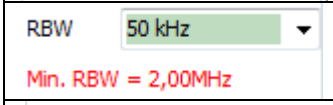
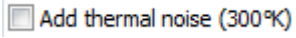
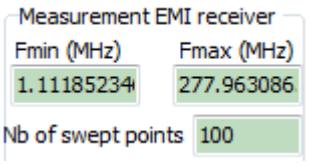
IV.6.3.3 Tab "FFT Parameters" - EMI receiver mode

Select the tab "EMI receiver" to choose the EMI receiver mode. In this mode, the effect of the IF filter of an EMI receiver followed by a peak detector is simulated. Thermal noise is also added to the simulated signal. The user adjusts two set of parameters:

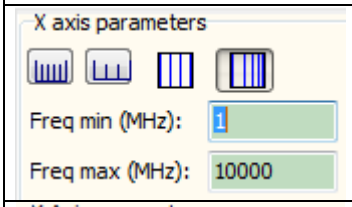
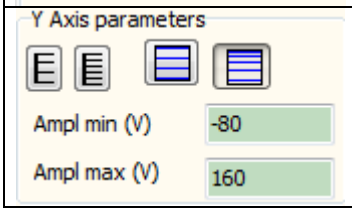
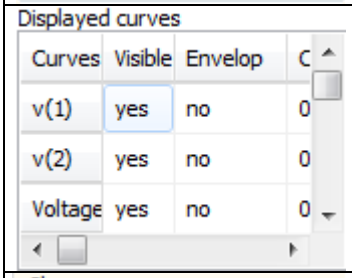
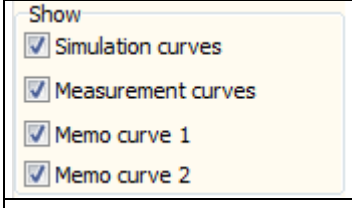
- the frequency sweep (min, max frequencies and number of frequency points). Depending on the number of points of the transient signal and the number of frequency points, the computation time may take several minutes. The frequency sweep may be chosen equal to the RBW.
- the resolution bandwidth (RBW) of the IF filter. The larger the RBW, the worst the frequency resolution and the noise floor is. A minimum RBW must be set to ensure a valid result. The minimum RBW value is given by the following equation, where Tmax is the duration of the transient signal. If this condition is not ensure, the amplitude of the computed spectrum is underestimated and the message "Uncal" will be displayed in the message bar of the screen.

$$RBW > \frac{1}{T_{\max}} \quad \textit{Equ. IV-1}$$

Buttons	Description

	Frequency sweep for the simulation results: the minimum frequency (Fmin) and maximum frequency (Fmax) of the EMI receiver. The number of frequency points are given by "Nb of swept points".
	Set the RBW of the IF filter. RBW values range from 10 kHz to 10 MHz. The message "Min. RBW" gives the minimum value of the RBW to ensure a valid computation.
	Add thermal noise to simulated transient signal. The thermal noise power is given by: $RBW = kT.RBW$ Where k is the boltzmann constant, T is the ambient temperature (300 K).
	Frequency sweep for the measurement results: the minimum frequency (Fmin) and maximum frequency (Fmax) of the EMI receiver. The number of frequency points are given by "Nb of swept points". These parameters are visible only if a .tran signal has been imported.
	Compute the response of an EMI receiver with the imported simulated and measured transient signals.

IV.6.3.4 Tab "Display"

Buttons	Description
	Adjustment of the X axis (frequency expressed in MHz). Click on the buttons or to enlarge or reduce the axis scale. Click on the buttons or to set a lin. or log. scale. The frequency bounds can also be manually with "Freq min (MHz)" and "Freq max (MHz)".
	Adjustment of the Y axis (voltage expressed either in V or dBµV). Click on the buttons or to enlarge or reduce the axis scale. Click on the button to set a lin. scale (in V). Click on the button to set a log. scale (in dBµV). The amplitude bounds can also be manually with "Ampl min" and "Ampl max".
	The table Displayed curves displays all the plotted spectra. The column "Curves" gives the name of the curve. In the column "Visible" , the user can change the visibility property for each curve through a pop-up menu. The envelop of a spectrum curve can be plotted if the property Envelop is set to Yes in the column "Envelop". Finally, the color of each curve may be changed by clicking on the last column "Color".
	Four groups of curves can be displayed: from simulation or measurement, and two memorized curve (Memo1 and Memo2). The visibility of each group can be modified with this menu.
	Store a curve in Memo1 or Memo2. First, select one curve in the table "Displayed Curves" by clicking on the corresponding row.

	Then, click on the button 1 to store in Memo1, or 2 to store in Memo2.
Remove	Remove one plotted spectrum curve. First, select one curve in the table "Displayed Curves" by clicking on the corresponding row. Then, click on the button Remove to suppress this curve.
Redraw	Redraw all plotted curves with default axis settings.

IV.6.3.5 Tab "Simu Data" and "Meas Data"

Buttons	Description
Input data / FFT Parameters / Display / Simu Data Freq (Hz) | v(1) (dBµV) | v(2 2,000M | -49,743 | -53 4,001M | -46,389 | -50 6,001M | -49,743 | -53 8,002M | -18,073 | -24 10,002M | -2,232 | -8, 12,003M | 2,270 | -3, 14,003M | -2,232 | -8, 16,004M | -18,101 | -24 18,004M | -54,202 | -56 20,005M | -51,717 | -54	The table in "Simu Data" Tab lists all the points of the displayed simulation curves. The table in "Meas Data" Tab lists all the points of the displayed measurement curves.

IV.6.3.6 Tab "Envelops & Limits"

Buttons	Description
Envelop parameters Nb points for envelop extract: 6	Parameter for extraction of spectrum envelop.
Save Envelop	Save the spectrum envelop.
EMC Limit Show limit Select emission limit: IEC61967-4 - 1 ohm Select category: Global-Class I Unit: dBuV Peak detector	Select an emission limit and its category. The category defines the severity class of the limit. The unit and the configuration of the EMI receiver are written below the list "Select Category". Click on "Show limit" to plot the emission limit.

IV.6.4 Near-field scan

The command "**EMC > Near-Field Scan**" gives access a specific screen for comparing measured and simulated near-field scan. The simulation file used for simulation is the result of a time-domain simulation where one or more inductances or interconnects are assigned physical coordinates. The time-domain simulation result is the current flowing in each declared inductance. An FFT is performed on each current information I(t) to compute the corresponding I(f).

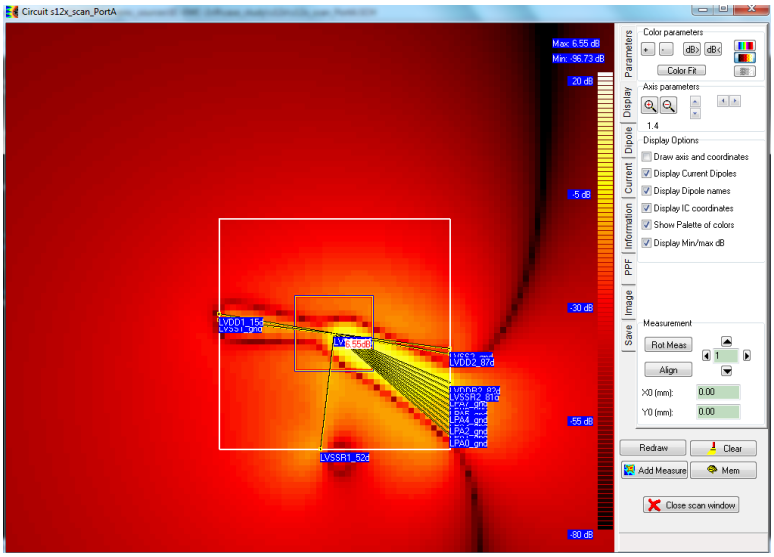
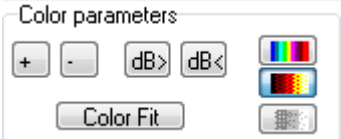
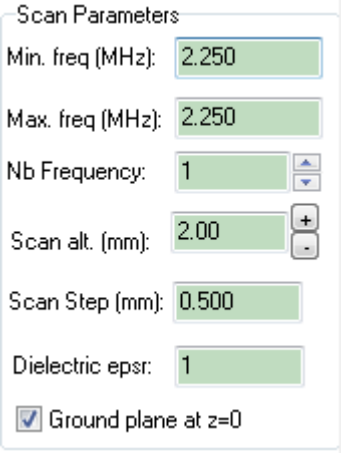
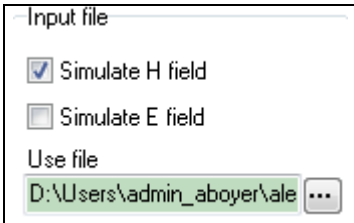
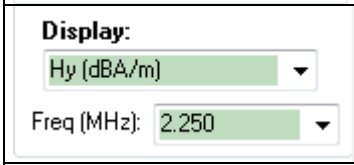


Figure 4- 22:The near-field scan user's interface (case_study\s12x\s12x_scan_portA.sch)

Each inductance is associated a radiating current element that is represented in the [x,y] plan as an elementary line (Figure 4- 22).

IV.6.4.1 Control Buttons

Buttons	Description
	Zoom and shift the near-field scan information
	Adjust the color palette, change the display mode from color to gray levels.
	Switch from measured to simulated scan. When clicking "simulate scan", the EM field is recomputed for all declared current elements, at the given frequency and given altitude.
	The near-field simulation may concern the total magnetic and electric fields Htotal and Etotal, and also one of their components in cartesian coordinate system (along x, y and z axis). The scan altitude may be changed. Click again "Simul. Scan" to recompute the new scan. The frequencies of interest may also be changed: the min and max frequencies are set and the number of frequency points. Once the new frequency has been fixed, click "Simul. Scan". The new *I(f)* will serve for the scan simulation. The scan step changes the computation step. As the scan area is set to 150 mm per 150 mm, for a 0.5 mm scan step, near field is computed at 90000 points. An infinite perfect ground plane can be added below the IC at Z=0. "Dielectric epsr" defines an overall insulator medium which may affect electric field distribution.

	Select the scan simulation file which include the current I(t) (*.txt) for each current element associated to each “radiating inductance” or “radiating interconnect” involved in the scan simulation and the voltages at each terminals of inductances. Check the box “Simulate H field” and “Simulate E field” to enable either H field or E field simulation.
	Select the E or H field component to display (x,y,z, tangential and total field component) at the frequency given in the field "Freq (MHz)". Magnetic fields are plotted in dBA/m and electric field in dBV/m.
	Add a measured scan. Three ways to described measured scans are supported by IC-EMC: 1. The proposed standard format in XML (.XML) 2. A basic text file containing a XY array of near-field values (.xy) See Chapter VI for more details about these formats

IV.6.4.2 Scan Difference

Several scans can be compared using embedded mathematical operations in the “Display” list in the "Parameters" menu. The results shown below concerns the subtraction of two magnetic field scans, one from simulation and one from measurements. The steps are as follows:

1. The first scan is loaded and stored in memory (Button “Memory”)
2. The second scan is loaded. By a click on “Active-Memory (abs)”, the absolute difference between the active XML scan and the memorized scan appear. The formulation is as follows, for each [x,y] point.

$$difference[x,y] = active[x,y] - memory[x,y]$$

3. An alternative subtraction may be performed based on weighted difference. The algorithm is as follows:

$$weight[x,y] = (\max(active[x,y], memory[x,y]) - dB\min) / (dB\max - dB\min)$$

$$result[x,y] = weight[x,y].difference[x,y]$$

Where

dBmin is the minimum value of the active scan data

dBmax is the maximum value of the active scan data.

IV.6.4.3 Other features

- You may add radiating elements using the right button of the mouse.
- When clicking on the [x,y] plane, the value in dBµV at the cursor location is added to the picture
- In the “Current” sub-menu, you may observe the time-domain and frequency domain of the current for each declared current element

- The scan may be configured using a text placed anywhere in the design, starting by keyword '.SCAN'. The format of this line is: ".SCAN step start_freq stop_freq freq_nb scan_alt dipole_alt". The six parameters that can be listed are given below (Figure 4- 23).

.SCAN	Scan configuration	.scan 0.5e-3 1e8 2e8 2 3.5e-3 1.2e-3	Scan step (1e-3), start frequency (100 MHz), stop frequency (200 MHz), number of frequency points (2), scan altitude (3.5 mm) and dipole altitude (1.2 mm)

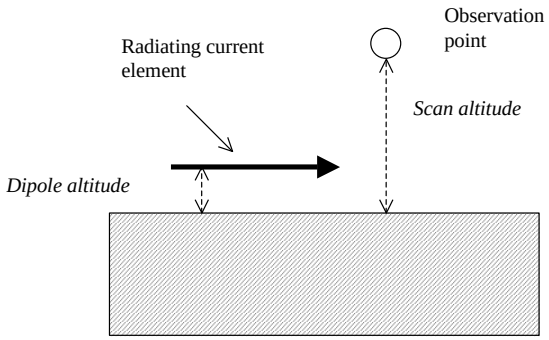


Figure 4- 23: The radiating element, its altitude and the scan altitude

IV.6.5 Susceptibility dBm vs. Frequency

The command "**EMC > Susceptibility dBm vs. Frequency**" gives access to a screen dedicated to susceptibility simulation control and susceptibility level extraction. A detailed example is given in part III.4. Figure 4- 24 presents the user interface of this tool, composed of two screens:

- the left part is dedicated to the control of the susceptibility simulation (parameters of the RFI source, definition of the susceptibility criterion, parameters of susceptibility threshold extraction). This screen proposes three tabs corresponding to the two simulation modes: "Manual", "Automatic" and "List". The difference between these modes is linked to the frequency sweep.
- the right part plots either the transient profile of the signal used as susceptibility criterion, or the extracted susceptibility threshold, given in term of dBm vs. frequency.

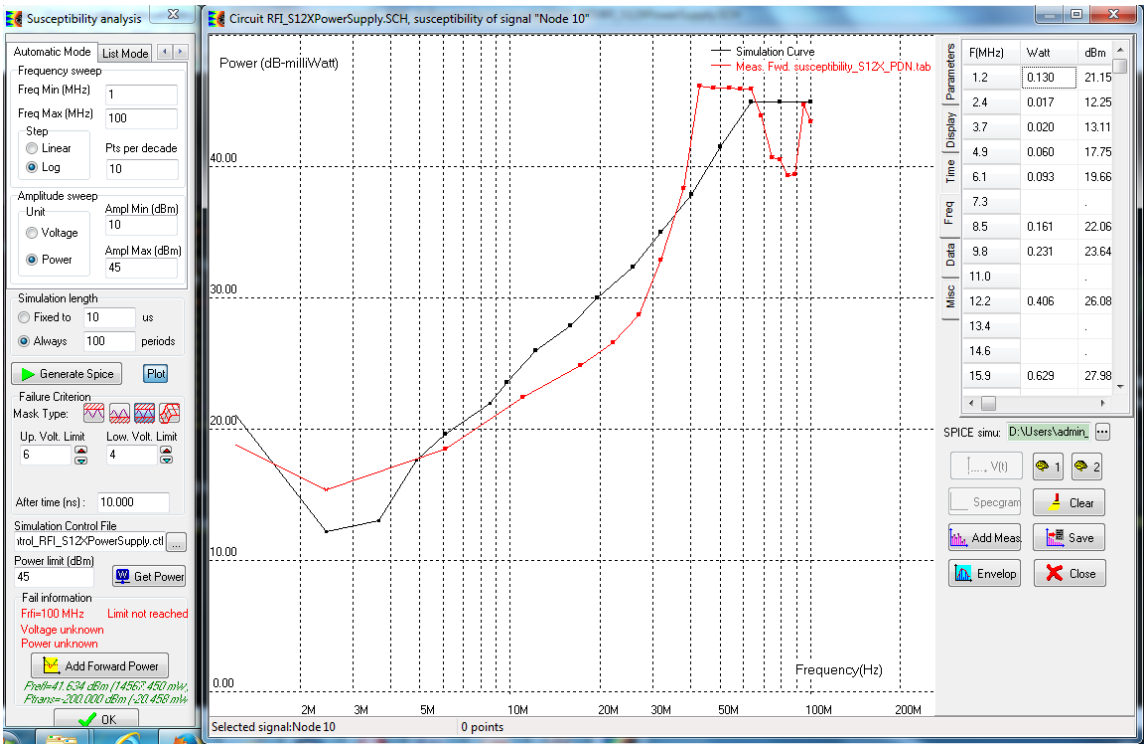
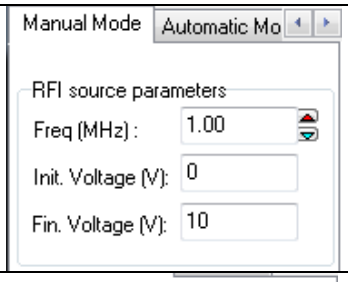
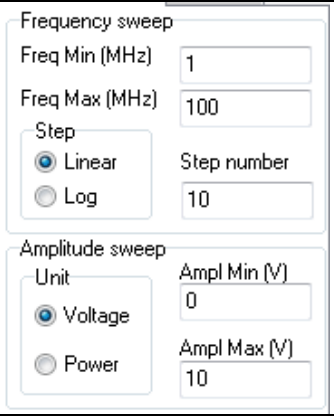
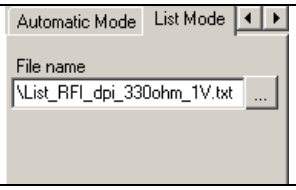
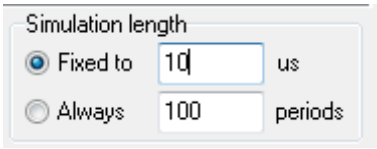
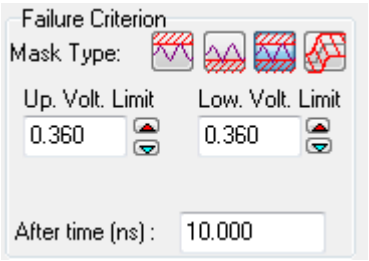
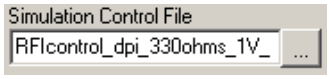
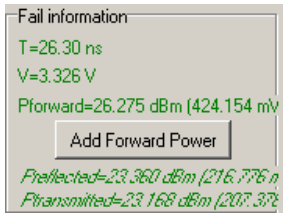
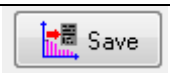


Figure 4- 24: The immunity simulation screen

First, configure the RFI and the SPICE simulation. Then generate the SPICE netlist and launch the SPICE transient simulation. At the end of the simulation, configure the susceptibility criterion and extract the susceptibility threshold.

IV.6.5.1 Control Buttons

Buttons	Description
	Control of the RFI source in Manual mode. Set the frequency of the RFI source, the start and stop amplitude of the RFI source. The amplitude can be defined in term of voltage (V) or power (dBm) depending on the option “Unit”. The voltage defines the amplitude of the voltage source included in the RFI source, so that it does not define the output voltage of the RFI source. The power defines the maximum available of the RFI source. It represents the power provided by the source to a matched load.
	Control of the RFI source in Automatic mode. This screen is split in two parts: Frequency sweep and Amplitude Sweep. First, set the frequency range of the RFI source: the start and stop frequency and the number of frequency points. The frequency sweep is linear. Then, set the the start and stop amplitude of the RFI source. The amplitude can be defined in term of voltage (V) or power (dBm) depending on the option “Unit”. The voltage defines the amplitude of the voltage source included in the RFI source, so that it does not define the output voltage of the RFI source. The power defines the maximum available of the RFI source. It represents the power provided by the source to a matched load.

	Control of the RFI source in List mode. All the configuration of RFI source, the transient simulation duration and the susceptibility voltage criterion for the different RFI frequencies are defined in a tabulated text file. See immunity\dpi330ohm \List_RFI_dpi_330ohm_1V.txt as example.
	Configuration of the SPICE transient simulation. The simulation length is set in term of time (case “Fixed to”) or RFI periods (case “Always”). This second option is adapted in automatic simulation mode when the simulation covers a large frequency range. If a fixed simulation duration is used for every frequency, this duration can be too short for low frequencies and too large for high frequencies. Click on the button “Generate Spice” to build the SPICE netlist of the susceptibility simulation.
	Configuration of failure detection. During RFI injection, a failure is associated to an abnormal state of a monitored signal. A mask is defined around this signal to detect a failure. The buttons defines upper, lower and upper&lower voltage limits for the monitored signal. These detection modes are suitable when a signal must not exceed a given voltage or remain in a given range. The button proposes a more complex detection, where both the amplitude and the period of the monitored signal must not deviate too much from those of a reference signal. It is necessary to define a mask around a reference signal with predefined amplitude and time margins. They can be defined in menu "Tools > Mask generator".
	This field appears only in automatic mode to import simulation result files. WinSPICE exports transient simulation results in .txt file for each frequency of the RFI. In automatic mode, a large number of .txt files are generated. A simulation control file .ctl is used to locate all the simulation result .txt files.
	The field “Power limit (dBm)” set a default power value if the failure criterion is not detected during a transient simulation. If the simulation is compared to a susceptibility measurement, this limit should be equal to the power limit in measurement, due to the limitation of the power amplifier. Click on the button “Get Power” to extract the susceptibility threshold. On the right screen, the transient profile is plotted to show the time when the failure is detected.
	Information of susceptibility threshold extraction process is indicated here. In manual mode, the time, the voltage, the forward, reflected and transmitted power when the failure appears is written. In automatic mode, the same information is written but only for the last frequency point. Click on the button “Add Forward Power” to add a new point to the susceptibility threshold in Manual mode, or to plot the extracted susceptibility threshold in Automatic mode. Click on the button “Save” on the right screen to save the extracted forward power. Click on the button “Add Meas.” to add a measurement. Measurements of susceptibility threshold are imported in .tab file (see Appendix A).
	Click on "Add Meas." button to display an immunity measurement results in a .tab text file. The file must contain one column with frequency and at least one column with the power required to induce a failure.
	Click on "Save" button to save immunity simulation results in a text file (.txt, .tab).

IV.6.6 Voltage Versus Time

The command “EMC > Voltage vs. Time” gives access to the time-domain waveform of the signal under investigation (Fig. Figure 4- 25). Simulation and measurement files are selected by clicking on ... in "Simulation Data" or "Measurement Data". Select the simulated or measured signal in the fields "Signals" and then click on the buttons "Add Simu" or "Add Meas" to plot it.

The X axis (time) and Y axis (volt) may be modified using the icons in the tab "Display". Click on the button "Auto Fit" to adjust the scale to include all the waveform, or define your own boundaries to zoom at a particular place. Click “FFT” to display the frequency-domain aspect of the wave, and “Spectrogram” to display the short-term FFT. Several properties of the signal can be analyzed depending on the quantity selected in the box "Quantity". Several quantities are related to each signal: amplitude, period, frequency, rise/fall time, jitter, duty cycle. Either their time-domain evolution or their statistical distribution can be plotted depending on the selected options in "Display mode". Part IV.6.6.2 describes the proposed analyses.

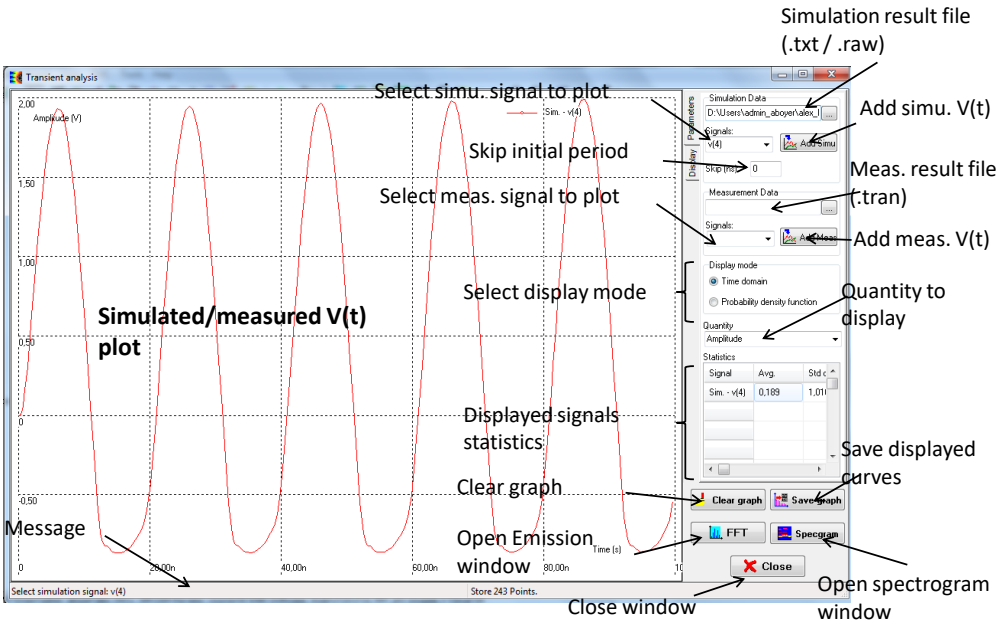
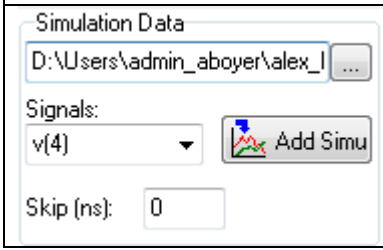
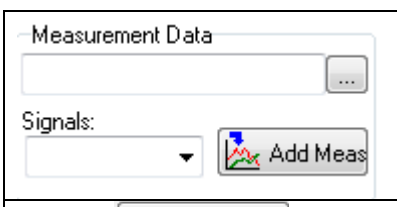
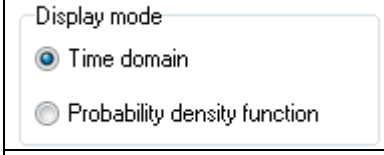
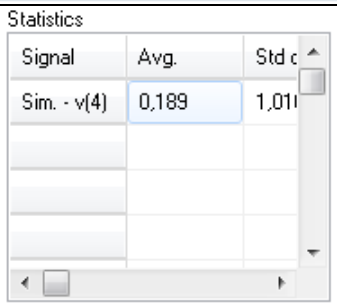
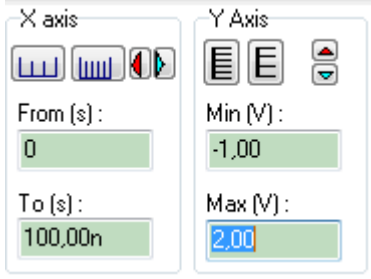
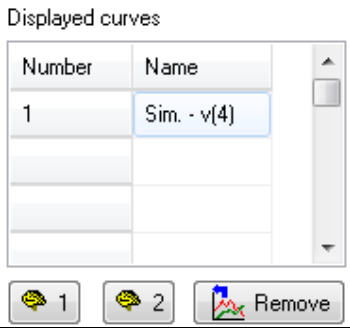
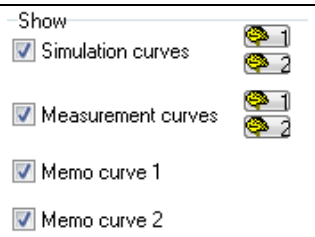


Figure 4- 25:Time-domain profile of the signal under investigation (case_study\s12x\s12x_RFI_pt3_iosupply_tran.sch)

IV.6.6.1 Control Buttons

Buttons	Description
	Select simulation file result with button ..., select the signal to be displayed in the box "Signals". Click on the button "Add Simu" to plot it. Remove the initial period of the signal with the field "Skip (ns)".

	Select measurement file result with button ..., select the signal to be displayed in the box "Signals". Click on the button "Add Meas" to plot it. Measurement file can be in .tran format.
	Clear the graph. All the displayed curves are removed.
	Save the displayed curves in a text file.
	Display the FFT or the short-term FFT (spectrogram) of the signal.
	Several quantities are related to each signal: amplitude, period, frequency, rise/fall time, phase/period/cycle-to-cycle jitter, duty cycle. Select the quantity of both simulated and measured signals to be displayed.
	Display mode selection. If the option "Time domain" is selected, the evolution in time domain of the selected quantity is plotted. If the option "Probability density function" is selected, the statistical distribution of the selected quantity is plotted.
	The table "Statistics" summarizes the statistical properties of the displayed quantities (average value, standard deviation, min. and max. values, number of occurrences).
	Adjust X and Y axis settings.
	Zoom options and auto-fit of the graph.
	List of displayed signals. Selection of curves to be stored (in memory 1 or 2) or removed.

	Show or hide simulation, measurement or stored (memo.) curves.

IV.6.6.2 Signal analysis

The following quantity of a signal can be extracted:

- amplitude (the default quantity when the tool is opened)
- period and frequency
- rise and fall time
- duty cycle
- phase jitter, period jitter and cycle-to-cycle (C2C) jitter

The tool offers two types of signal representation:

- Time domain: the transient evolution of the signal's quantity is displayed. This mode is interesting to track the evolution of one characteristic of a signal. For example, Figure 4- 26-top shows the evolution of output voltage of an inverter whose power supply is noisy. In the box quantity, select "Period" to plot the evolution of the period of the output signal of the inverter. The result shows that the period is not constant due to power supply voltage fluctuations.
- Probability density function: the statistical distribution of the signal's quantity is displayed. For example, the histogram shown in Figure 4- 27 describes the statistical distribution of the output voltage of a noisy inverter. The histogram gives the probability density function of a random variable, which is the output voltage here. The table "Statistical properties" provides the minimum, maximum and average values, the standard deviation of this random variable and the number of occurrences used to extract this histogram.

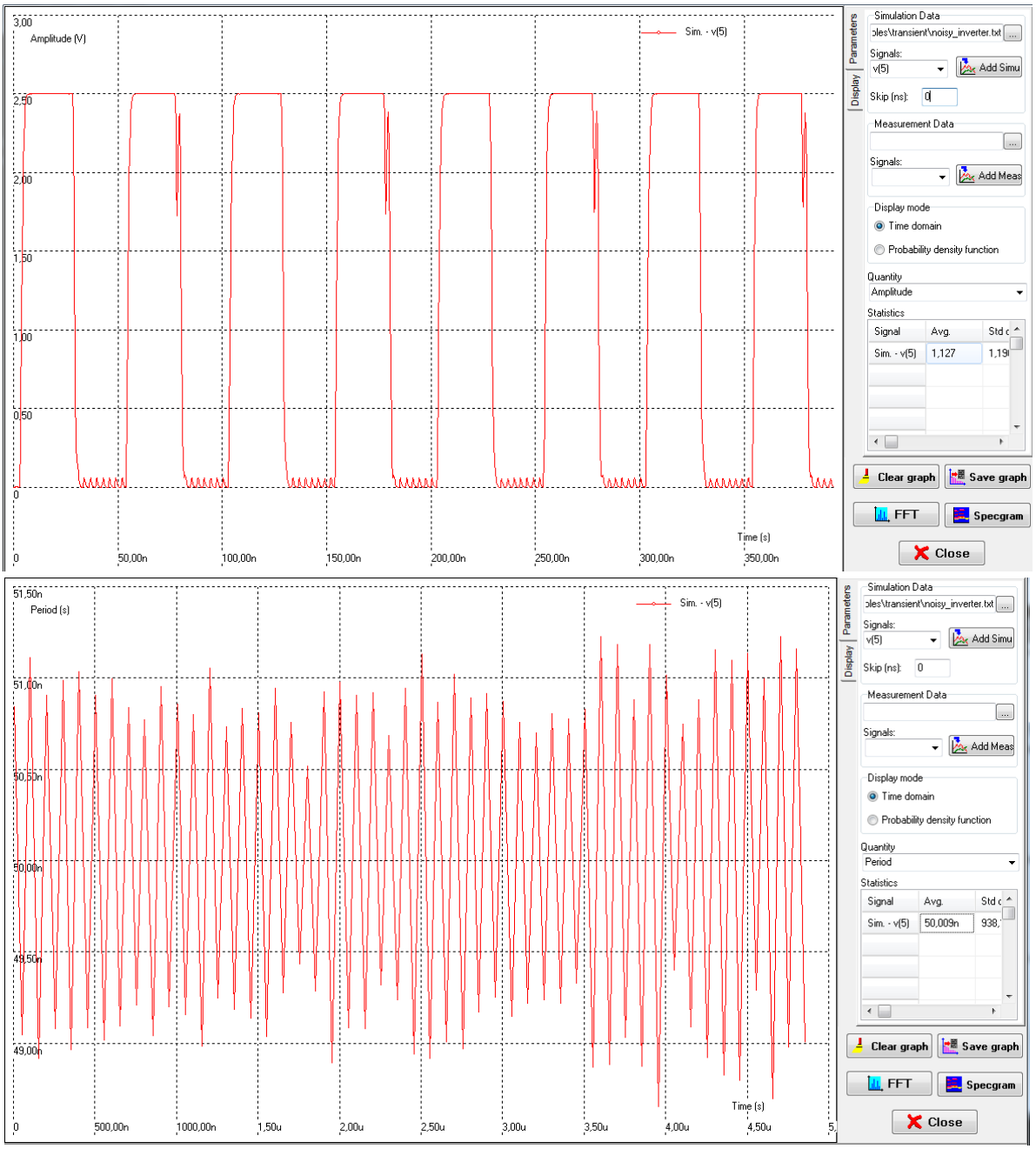


Figure 4- 26: Output voltage of a noisy inverter (top), and tracking of the period of its output signal (bottom) (\examples\transient\noisy_inverter.sch)

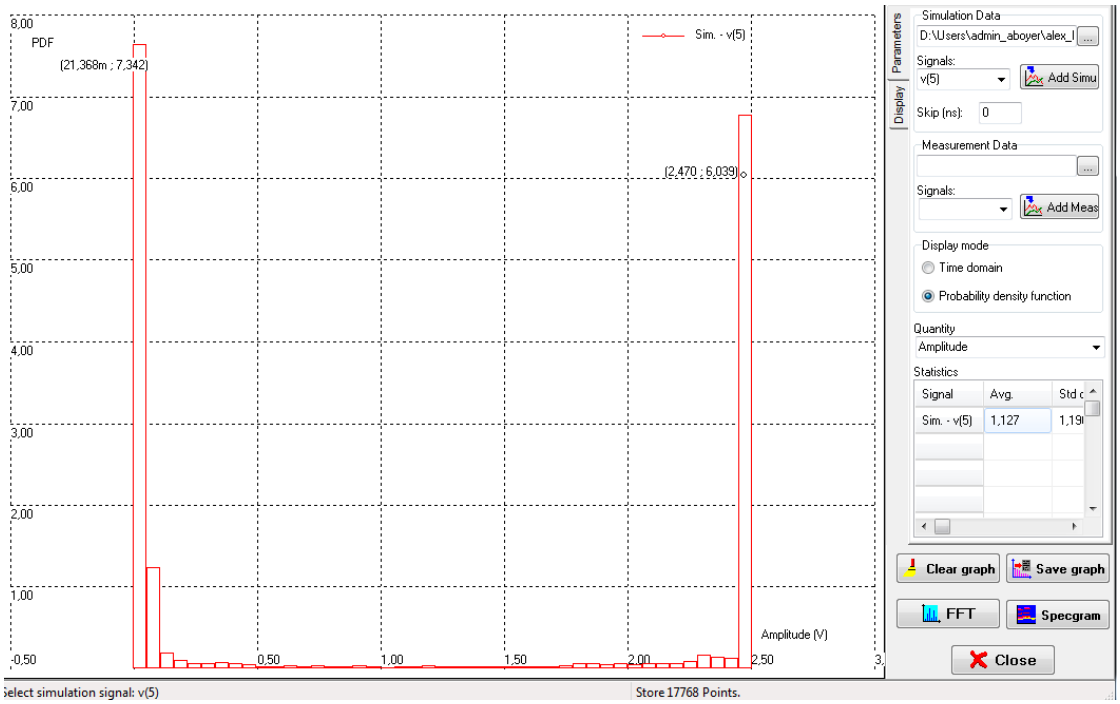


Figure 4- 27: Statistical distribution of the amplitude of the output voltage of a noisy inverter (\examples\transient\noisy_inverter.sch)

IV.6.7 Impedance vs. Frequency

The command "EMC > Impedance vs. Frequency" gives access to a specific screen for comparing measured and simulated impedance versus frequency. The simulation file is the result of a small-signal frequency-domain simulation (AC simulation) controlled by a single Z probe placed on one port of the device under test. For multiport analysis, refer to S parameter analysis (part IV.6.8).

Figure 4- 28 shows the screen “Impedance vs. Frequency”. The simulation of the impedance seen between power supply and ground pins of a microcontroller are compared with a measurement results. The X and Y axis may be modified using the icons situated on the top-left corner of the screen.

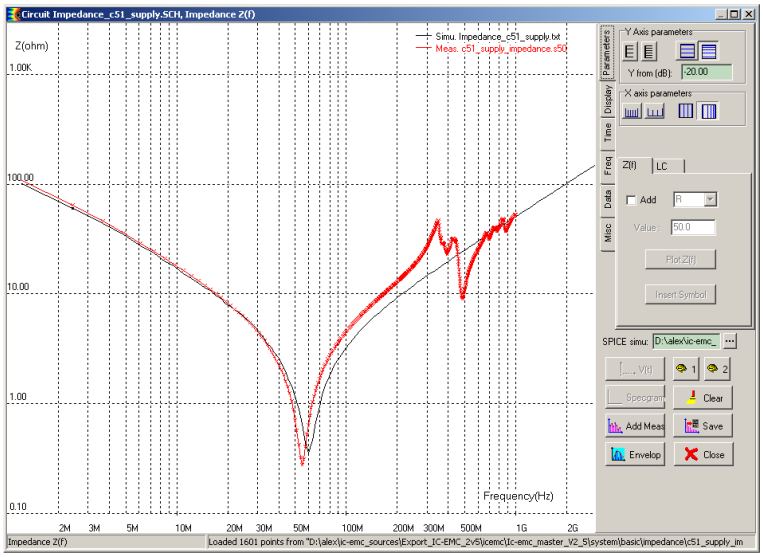
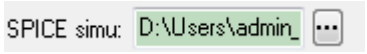
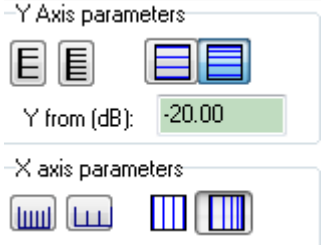
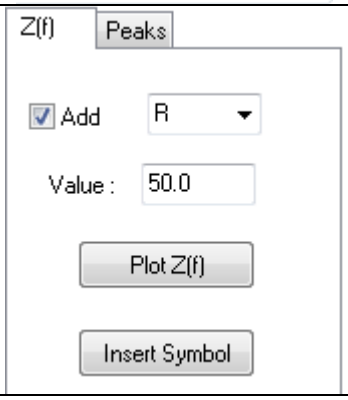
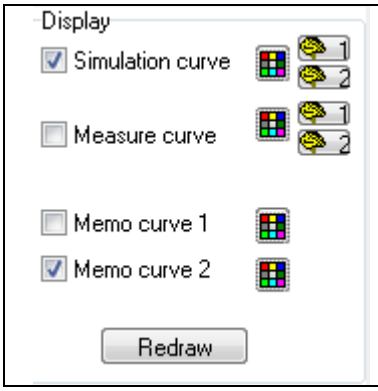


Figure 4- 28: The Z(f) screen with frequency-domain simulations (\examples\impedance\Impedance_c51_supply.sch) compared to measurements (\examples\impedance\c51_supply_impedance.s50)

IV.6.7.1 Control buttons

Buttons	Description
	Select simulation file result with button ... . Only one simulation curve is plotted. .
	Select measurement file and plot measured impedance profile in frequency domain. Input file are in .z, .s50 and .s1p format.
	Clear the graph. All the displayed curves are removed.
	Save the displayed curves in a text file.
	Store simulation and measurement curves (Memo1 and Memo2)
	Adjust X and Y axis settings.
	Plot the impedance profile of ideal passive device (seect Add, select device, fill "Value" and click on "Plot Z(f)". A component can be placed on schematic by clicking on the button "Insert Symbol".

	Show or hide simulation, measurement or stored (memo.) curves.

IV.6.8 S parameter analysis

The command "EMC > S parameters" opens a specific screen for comparison measured and simulated S parameters. The simulation result file is the result of an AC simulation where one or more ports have been defined. They can be converted in Z parameters. The S parameters between each of these ports are computed at each frequency defined by the AC simulation. S parameter simulations and measurements are limited to 4 active ports and 4000 frequency points. By default, single-ended port representation of S or Z parameters are used, i.e. forward and backward waves at each port are defined between a terminal and a common reference. For problems where common-mode and differential mode characterization is necessary , it can be convenient to use a mixed-mode representation. The reader can refer to [Boc95] for more information about mixed-mode S or Z parameters and conversion formula between single-ended and mixed-mode S or Z parameters. Mixed-mode representation is proposed only for 2 or 4-port models or measurements.

The simulation results are written in several .txt files associated to a given S parameter (for example S11_file_name.txt). The parameters of the simulation and the result file names are listed in a *.spc file. Figure 11-36 shows the screen “S Parameter Analysis”. The simulation file is chosen in the field “Simulation Data Source”, the list of simulated S parameters appears just above in the list “S parameter”. Different values associated to S parameter can be selected in the list “Value”:

- Magnitude in linear scale “Mag (linear)”
- Magnitude in dB “Mag (dB)”
- Real part of the magnitude “Mag (real)”
- Imaginary part of the magnitude “Mag (imaginary)”
- Phase in degree “Phase (degree)”
- Phase in radian “Phase (radian)”

Click on button “Add” to display the selected S parameter in the chosen format. The S parameter can be converted in terms of Z parameter by clicking in the checkbox “Z” in the “Conversion” field. X and Y axes can be set in linear or logarithmic format. S parameters can be displayed in a Cartesian graph (Amplitude vs. Frequency) or in a Smith chart.

Measurements can be imported in the field “S Parameter Measurement” in order to compare with simulation results. The S parameter data files are Touchstone file “*.snp”, where n is the

number of port. See Appendix A for more information about Touchstone file format. Click on the button “Add Meas.” to display the measurement results and compare them to simulation results. Click on the button “Save” to export simulation results in a standard Touchstone file.

If you click directly on the screen, the corresponding coordinate appear on the screen. If the curves are displayed in a Cartesian graph, the coordinates indicates the frequency and the value of the point on which the user have clicked. If the curves are displayed in a Smith chart, the frequency, the amplitude in linear and the phase in degree of the closest point of the closest curves are returned.

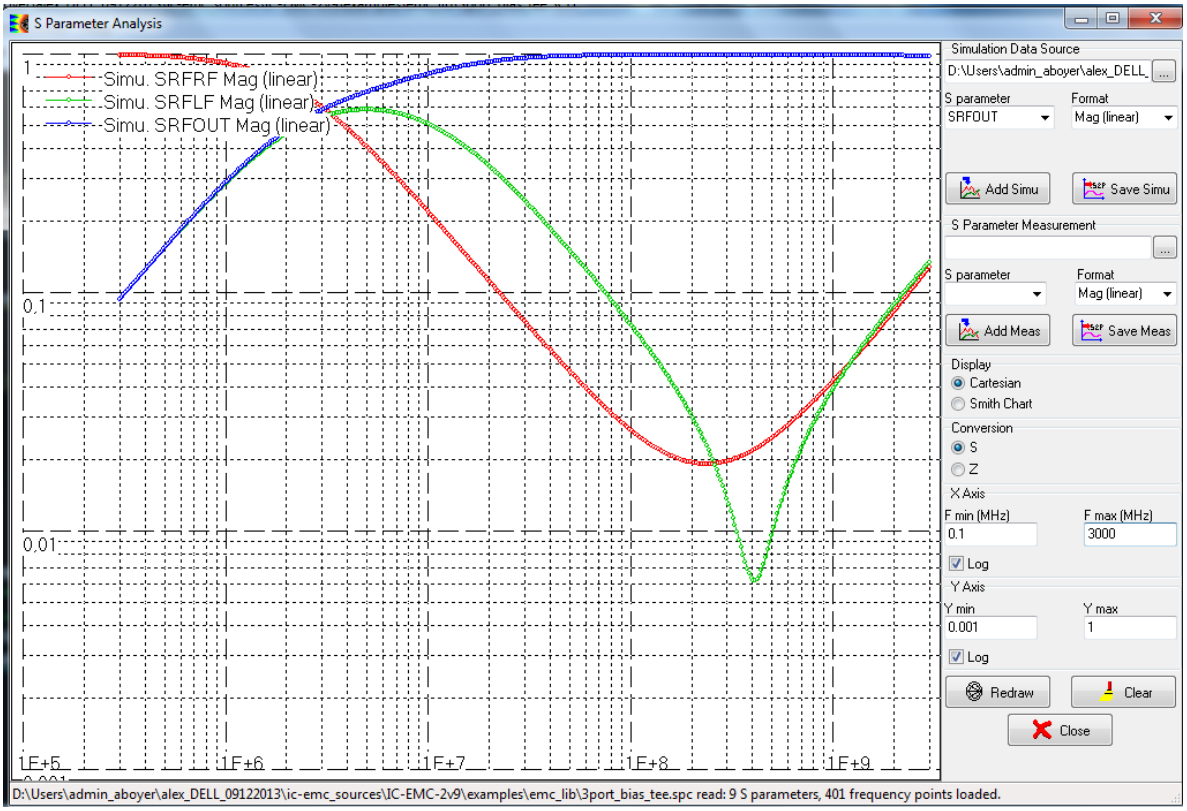
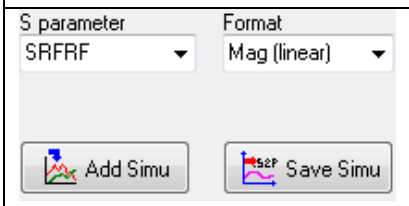
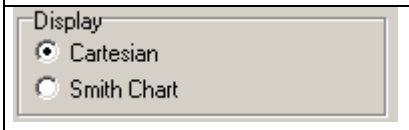
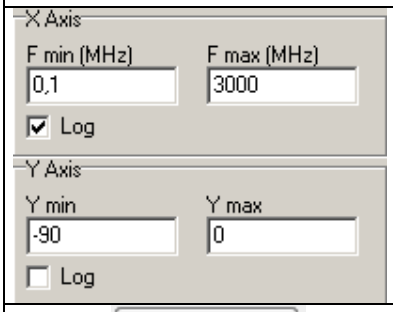
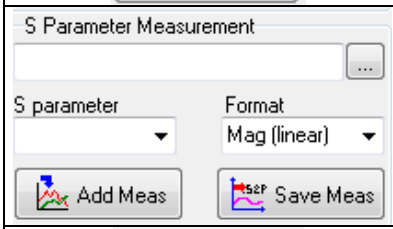


Figure 4- 29: S parameter analysis user’s interface (\examples\EMC_lib\3port_bias_tee.sch)

IV.6.8.1 Control Buttons

Buttons	Description
	Import the S parameter simulation control file *.spc. If a schematic corresponding to a S parameter simulation is opened, the associated .spc file is opened.
	Add a simulated S/Z parameter curve on the graph. Save all the simulated S/Z parameters in a Touchstone *.s*n*p file. The option “Conversion” sets the format of the parameters to be saved (S, Z, mixed-mode S or Z). The box “S parameter” lists all the S parameters between the N active ports defined in the schematic. The box “Format” lists the different format proposed by IC-EMC to display the S parameters: magnitude in linear or dB scale, real and imaginary part, phase in degree or radian.
	Display S parameters in a Cartesian graph or in a Smith chart. Suppose that several curves are displayed in a Cartesian graph. If you want to display curves in a Smith chart, click on the box “Smith Chart”, the previous curves are cleared. Then click on the button “Add” to display new curves in a Smith chart.

	Display simulated and measurement results in single-ended S or Z parameter format (box "S" or" Z"), or in mixed-mode S or Z parameter format.
	X and Y axes settings. The default settings are computed to display all the curves.
	Redraw all the curves after a change of axes settings.
	Add S parameter measurement results on the graph. the format of measurement is Touchstone file *.snp. Choose the measurement file, then choose the S parameter to display and its format and click “Add Meas” to display the measurement. Click on the button "Save Meas." to save the measurement results in the format displayed on the screen.
	Clear all the graphes.

IV.6.9 Parametric analysis

The command “EMC > Parametric analysis”  opens a screen for the configuration of a parametric analysis (Figure 4- 30).

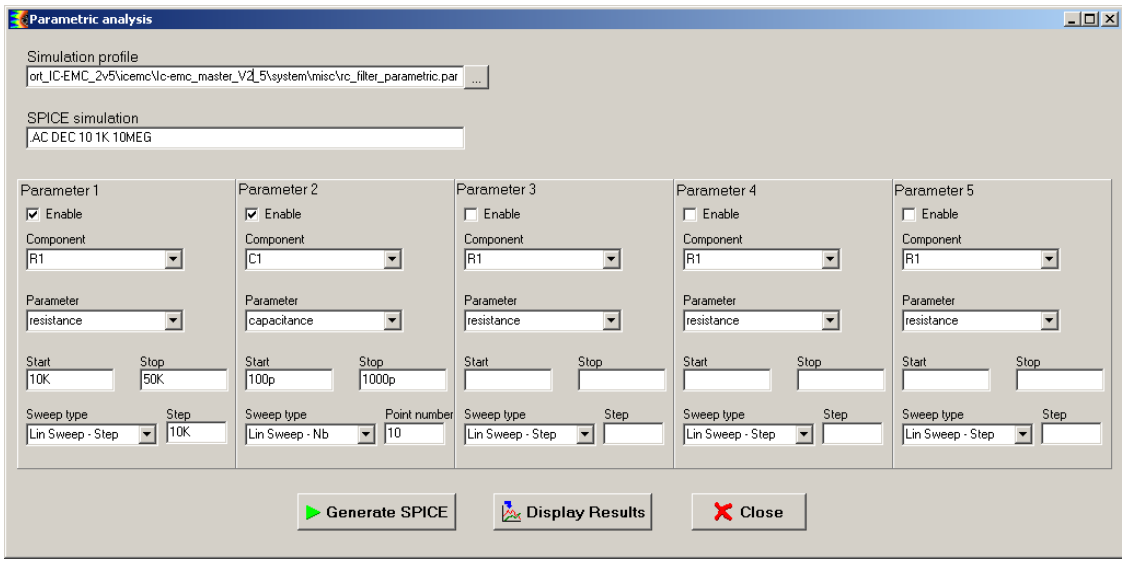


Figure 4- 30: Parametric analysis configuration interface (examples\misc\rc_filter_parametric.sch and examples\misc\rc_filter_parametric.par)

The parametric analysis consists in sweeping one up to five parameters of the devices inserted in the schematic (passive or active devices, sources, temperature, model parameters included in a library file (*.lib)). Select the option “Enable” to activate a parameter, select one component in the field ‘Component’ (e.g. the resistance R1 of the schematic ‘misc\rc_filter_parametric.sch’ as shown in Figure 4- 31) and one of its property in the field ‘Parameter’ (e.g. the resistance value). Then, define the sweeping with the start and stop value, the type of sweep (Linear or logarithmic sweep, number of step (‘Point number’ field) or value of the step (‘Step’ Field)). Once all the parameters have been configured, click on the button ‘Generate SPICE’. A simulation type has to be preconfigured or detailed in the field ‘SPICE simulation’. Only AC, DC and transient simulation are supported. Although S parameter, susceptibility, emission and near-field scan simulations rely on AC, DC or transient simulations, they are not supported by the Parametric analysis tool.

The parametric analysis configuration is saved in a *.par file, defined in the field ‘Simulation profile’. This file is required to find all the SPICE simulation result files corresponding to the sweep of the parameters. Each time the button “Generate SPICE” is clicked, the *.par file is updated. The name of the *.par must be the same as the schematic name (for example, for the schematic called ‘misc\rc_filter_parametric.sch’, the configuration of the parametric analysis is saved in the file ‘misc\rc_filter_parametric.par’). A pre-existing parametric analysis file can be imported by clicking on the button  .

At the end of the SPICE simulation, click on the button ‘Display Results’ to plot the simulation results vs. parameter values (Figure 4- 31). The parametric analysis configuration file *.par can be loaded in the field ‘Simulation Data Source’. Select the different parameter values and click on the buttons Add or Clear to add or remove simulation curves. The simulation curves can be saved in a *.txt file. Measurement can be loaded in a *.tab format.

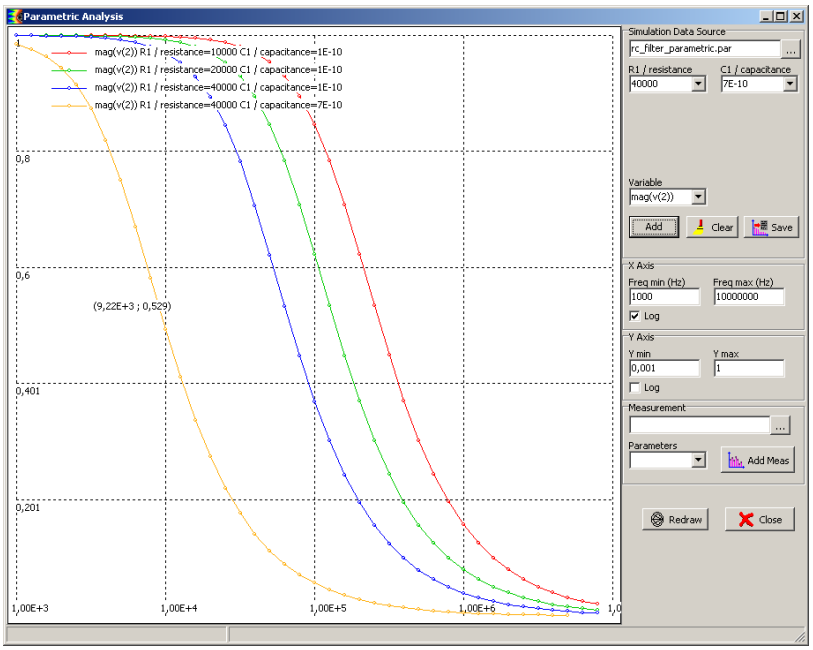


Figure 4- 31: Plot of the results of Parametric analysis (examples\misc\rc_filter_parametric.par)

IV.7 Detailed commands of Menu Tools

IV.7.1 ICEM Model Expert

Click “Tools > ICEM Model Expert” to access the interface reported below. This tool aims at building a simple IC emission model according to ICEM standard [ICEM] from basic information about the circuit. This type of analysis is particularly suited for evaluation of emission at pre-design stage or when an existing circuit is not available physically.

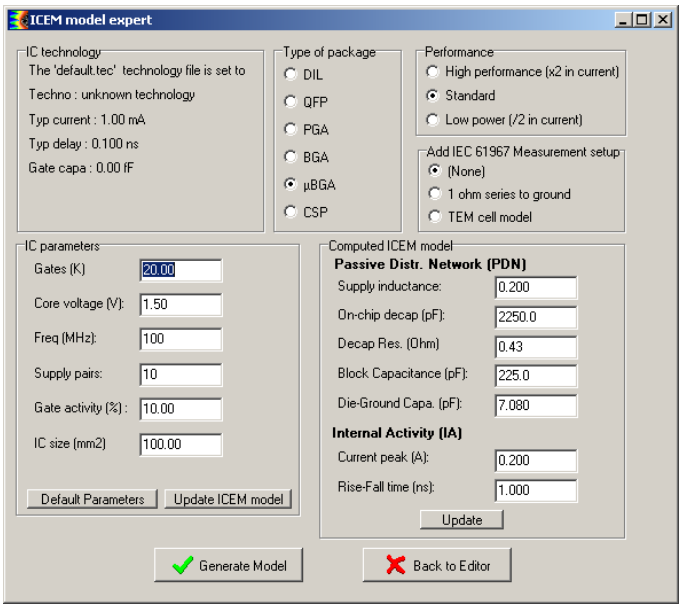


Figure 4- 32: The ICEM model generator and its user’s interface

On the left upper corner of the window, the default technological parameters are listed. These parameters are provided in the configuration file “default.tec”, which is described in part VI. The parameters worth of interest are:

- The typical switching current per gate (0.2 mA in 0.12 µm technology)
- The typical duration of the gate switching (50 ps in the above example)
- The default gate decoupling capacitance (5 fF)

The next menu, called “Type of package”, selects the family of package, which has a direct impact on package inductance. The “performance” menu tunes the current peak (Ib) by increasing the peak current by 100% in “high speed” mode as compared to standard mode. In “low power” mode, the current is reduced by 50%.

In the lower left corner, several parameters that have a direct impact on the ICEM model are given:

- The number of gates (20 Kgates by default)
- The core voltage (1.2 V by default in 0.12 µm)
- The operating frequency (100 MHz by default)
- The supply pairs (Number of VDD/VSS pins, 10 by default)
- The % of switching activity in each active edge of the clock (10% by default)

- The IC size in mm (10 x 10 mm by default)

The computation of the ICEM elements is performed using the approximations described in Table 4- 3. The button “Update ICEM Model” updates the proposed values for the Passive Distribution Network and the Internal Activity. The button “Generate Model” creates a simple schematic diagram from these parameters.

You may also add:

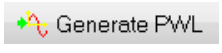
- A 1-Ω serial resistance on the ground path, associated with 50-Ω adaptation as defined in the IEC standard “1/150Ω conducted measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer.
- A capacitance/inductance coupling with the septum of the TEM cell, associated with 50-Ω terminations, as defined in IEC standard “TEM radiated measurement method”. A probe is placed at the location of the measurement system, usually a spectrum analyzer.

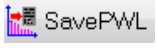
Ldie_vdd = sqrt(icSurface) *inductanceFactor; Rdie_vdd = sqrt(icSurface) *resistanceFactor;	The serial inductance and resistance values are proportional to the width of the die. The factors are around 0.1, if the IC size in in mm.
imax=icPerfo*Gates*typ_current* Gate_Activity/spreadFactor;	The peak current of the source Ib is computed using several parameters: the spread factor is around 10; icPerfo is equal to 2 for high performance, 1 for standard and 0.5 for low power option.
tr := typ_Delay*SpreadFactor;	The rise and fall time of the current source is multiplied by the spread factor.
Lpack_vdd :=L_package/SupplyPairs;	The serial inductance is divided by the number of pairs. The inductance per pin depends on the package technology (15 nH for DIL down to 1nH for CSP).
Cd := Gate_Capa*Gates+ icSupplyPairs*ioCapa+ icSurface*SurfaceCapa;	The decoupling capacitance is the sum of the gate capa, the Io capa and the die surface capacitance.
Cb := Cd/10	The local block capacitance Cb is 10 times lower than the total capacitance
defaultRcd = 1.0; // (Ohm) Decap_Res := defaultRcd/ln(icSupplyPairs)	A parasitic serial resistance is added to the decoupling capacitance to account for interconnect access to physical resistance.
Cdg:= eps0*icSurface*packEpsr /icAltitude;	The die-to-ground capacitance is computed using a simple surface capacitance formulation, given physical parameters such as the surface of the die, the relative permittivity of the package and the IC altitude to ground.
CxFactor = 1fF/mm^2; Cx:= CxFactor*icSurface;	For TEM cell coupling, we use a value Cx which accounts for the coupling between the silicon die and the septum plate, which is the order of 1fF/mm^2

Table 4- 3: Algorithm for ICEM model automatic generation

IV.7.2 PWL Source Generator

The Piece-Wise-Linear source generator ("Tools → PWL Source Generator") is a convenient way to build an arbitrary input waveform included in a voltage or current source for simulation. A powerful mathematical set of routines enables to describe virtually any waveform and transform it into a series of (Time,Voltage) points. Predefined waveform descriptions are proposed in the menu on the left ("Select the mathematical operation" part), based on a reduced set of parameters listed in the middle part ("Parameters"). The user can also manually edit the equation in order to obtain its own waveform.

Click on the button 

to verify the correctness of the mathematical expression and visualize the waveform profile in time domain (screen on the right). The output of this tool is a text file that is compatible with SPICE PWL source description. The path of the text file must be specified in the field "File name". Click on the button 

to select the output file and save the PWL points.

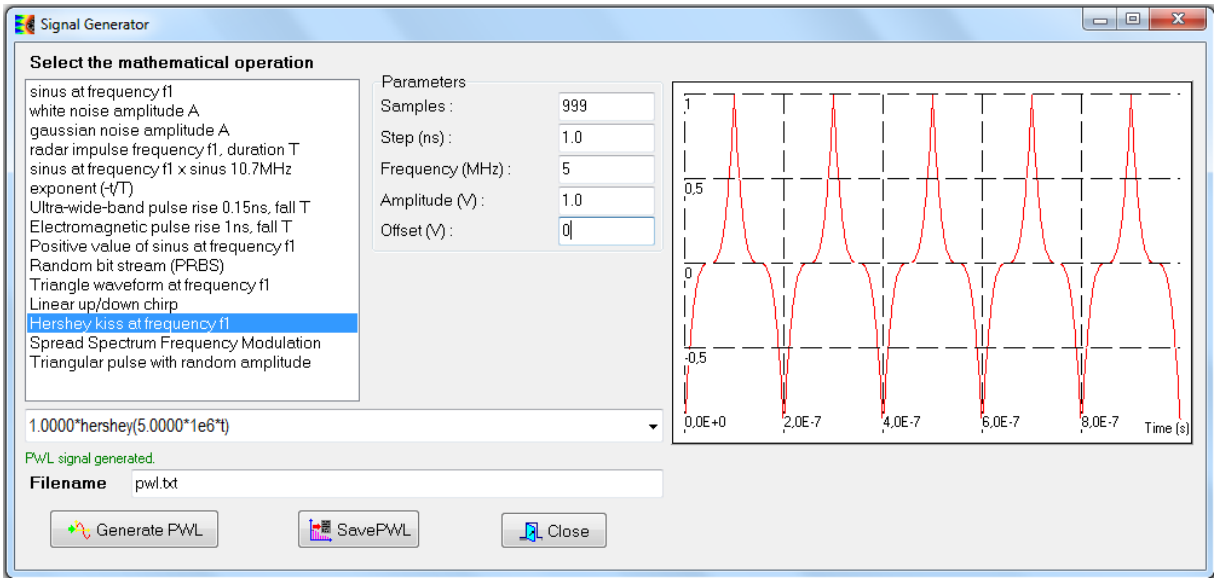


Figure 4- 33: PWL generator example

An example of output TXT file ("PWL.TXT" by default) is given below:

- `PWL description for 1.0000*exp(-t*/0.15e-9)-exp(-t*/100.0000e-9)`
  `+(0.0NS 0.0000 1.0NS -0.9888 2.0NS -0.9802 3.0NS -0.9704 4.0NS -`
  `0.9608 5.0NS -0.9512 6.0NS -0.9418 7.0NS -0.9324 8.0NS -0.9231`
  `+9.0NS -0.9139 10.0NS -0.9048 11.0NS -0.8958 12.0NS -0.8869 13.0NS`
  `-0.8781 14.0NS -0.8694 15.0NS -0.8607 16.0NS -0.8521`
  `...`

Number of samples and step of the PWL description are given by the fields “Samples” and “Step (ns)”.

IV.7.2.1 Mathematical functions

Function	Description
Abs	Absolute value
Arcos	Invert cosine
Arcsin	Invert sinus
Arctan	Invert tangent
Abs	Absolute value
Avg	Average of the signal
Cos	Cosine
CosH	Hyperbolic Cosine
Exp	Exponent
Gauss	Gaussian noise; the parameter is the variance
Int	Integral
Logic	Random logic value between VDD and VSS, changed at period given as a parameter.
Norm	Normal distribution
Pi	3.1415927
P2	2*pi
Pos	Positive value of the signal
RMS	Root mean square
Sin	Sinus
SinH	Hyperbolic Sinus
Sqr	Square

Sqrt	Square root
White	White noise; the parameter is the amplitude
t	Time in seconds
Tan	Tangent
Vdd	Voltage supply; given in the technology file
x	Time in seconds

IV.7.2.2 Function Examples

A user's defined equation may be entered to create virtually any type of waveform. Examples are given below. The full list of functions is reported in Table 4- 4.

Function declaration	**Function description**
10.0*sin(2*pi*100e6*t)	100 MHz sinusoidal wave, 10 V amplitude
white(3.0000)	White noise, amplitude 3 V
gauss(1.0000)	Gaussian noise, amplitude 3 V
10*exp(-sqr((t-100e-9)/100e-9))*sin(2*pi*1e9*t)	Radar pulse at 1 GHz, starting at 100 ns, 10 V amplitude
100*(exp(-t*/100.0e-9)-exp(-t*/0.15e-9))	Ultra-wide band pulse, 100 V amplitude (double exp)

Table 4- 4: Examples of function declaration

IV.7.3 Mask generator

The tool "Tools > Mask generator" aims at defining masks for failure detection during susceptibility simulation. A mask consists of an upper and lower limits defined around a reference signal, which is the response of a circuit under test in nominal regime. The distance between limits and the reference signal depends on amplitude and time margins predefined by the user. During a susceptibility simulation, each time the deviation between the response of the circuit under test in susceptibility test and its nominal response is larger than these margins, a failure will be detected during the susceptibility simulation.

Figure 4- 34 presents an example of a digital signal that switches periodically from a '0' to '1' level. It is the reference signal, imported by clicking on the button ... . Its amplitude is 2.5 V and its period is equal to 50 ns. Two types of failure may arise: an excessive amplitude deviation or transition time shift. In both cases, these signal distortions may lead to incorrect bit detection. A common detection method consists in deriving a mask whose upper and lower bounds are built from a reference signal plus or minus amplitude and time margins. If the monitored signal goes outside the mask when electromagnetic disturbance is injected, then a failure is detected.

The parameters to build the mask are:

- skip (ns): define the start time of the mask. It may start at t > 0 to avoid initial transient events on the reference signal which may produce false detection of failures.
- Time margin (ns): the maximum allowed period change. In this example, the time margin is set to 5 ns, i.e. +/- 10 % of the reference signal period.
- Voltage margin (mV): the maximum allowed voltage change. In this example, the voltage margin is set to 250 mV, i.e. +/- 10 % of the reference signal amplitude.

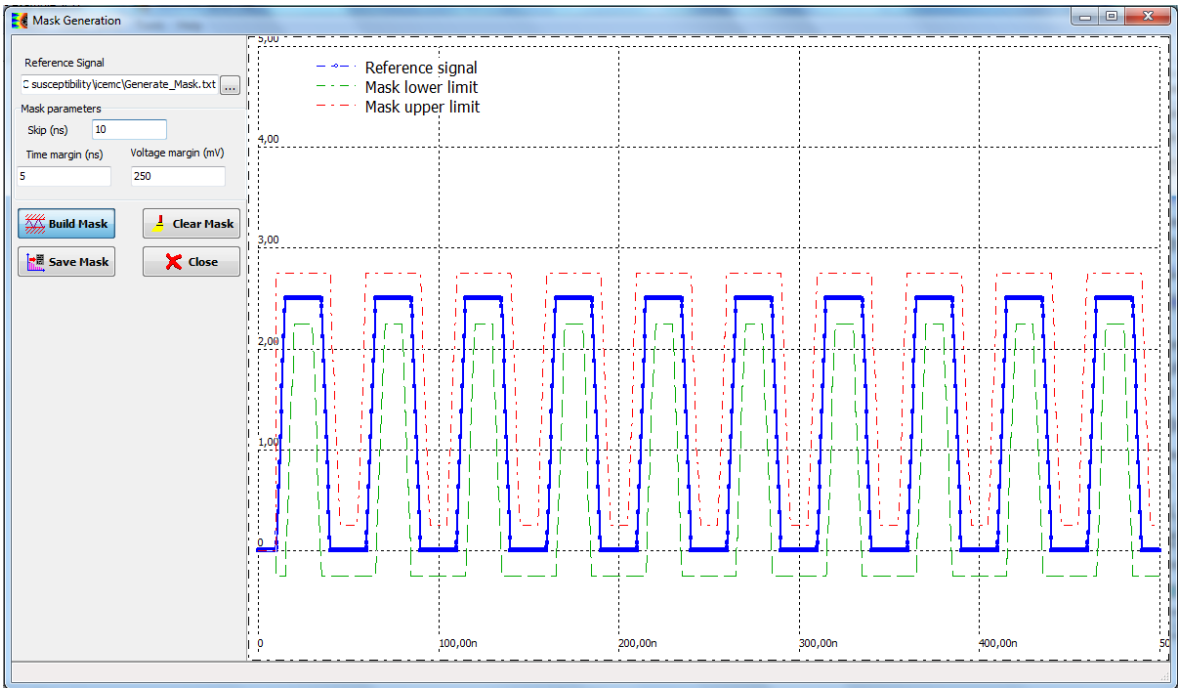


Figure 4- 34: Generation of a mask for failure detection during susceptibility simulation

Click on the button  to save the mask upper and lower bounds in a text file. This file will be imported during susceptibility simulation to detect failure, as explained in part IV.6.5.

IV.7.4 Advanced Spice & Ibis

The command “Tools > Advanced Spice & Ibis” is based on the IBIS data loaded in the schematic editor (see command "File > Load Ibis File"). It may be used to:

- Generate a symbol including the pin list and package shape (**Physical Symbol**)
- Evaluate the R,L,C values for each pin of the package based on physical estimation of the package lead length and bonding length (R,L,C distribution)
- Evaluate the mutual coupling (Mutual Coupling)
- Generate advanced IBIS netlist including accurate evaluations of packge and lead elements (IBIS netlist)
- Generate sub-circuit containing all R,L,C sub-elements in a Spice-compatible format (Spice Netlist).

Notice that the parameters displayed in the menu are issued from hidden IBIS parameters related to the physical dimensions of the IC, the package cavity and package size. An example of package model extraction is given in III.9.3.

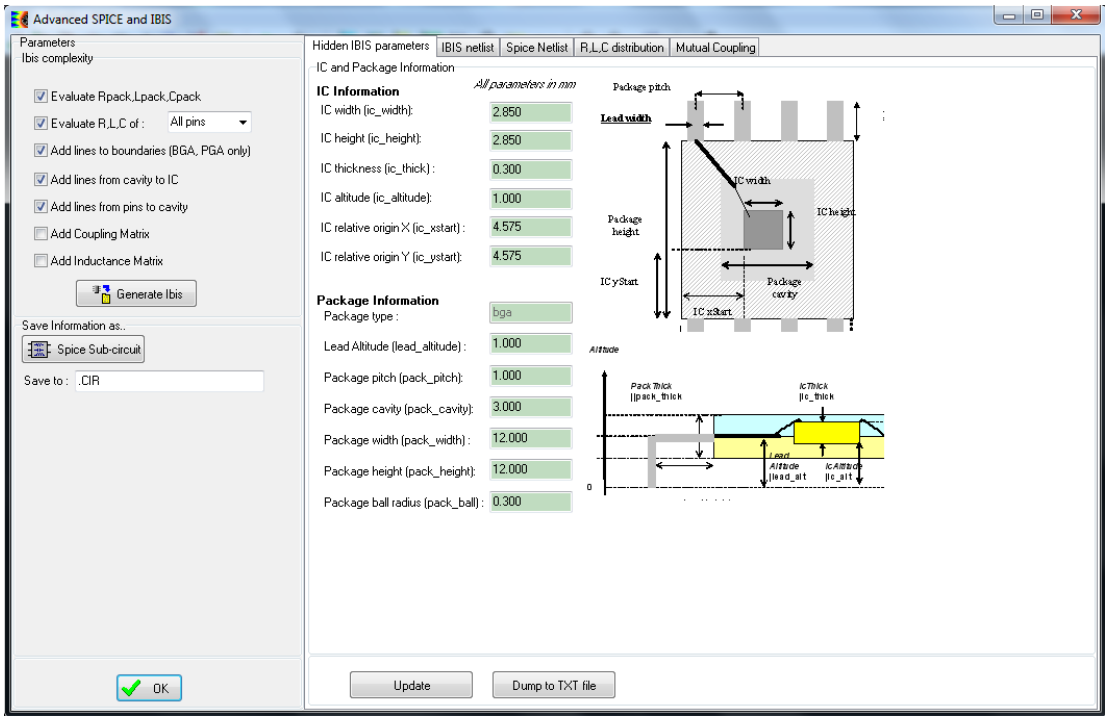


Figure 4- 35: the user's interface for the Advanced Spice and Ibis Information

IV.7.5 3D-Package Viewer

The package viewer is based on IBIS information of the integrated circuit. Use the command "Tools > 3D-Package Viewer" to display the 3D aspect of the package, including the IOs, IC location and lead-frame structure. When the 3D-package viewer is launched, the tool asks for a IBIS file. The "Demo" button displays the IC in 3D with varying observation angles.

Use the X, Y, Z to move the viewer's position in 3D and the light position cursor to change the rendering. The package color and the IC colors are user accessible. The color code for pins is as follows:

- Supply balls are in red (VDD, VCC)
- Ground balls are in blue (GND, VSS)
- I/O balls are in yellow
- Non-connected balls are in Gray

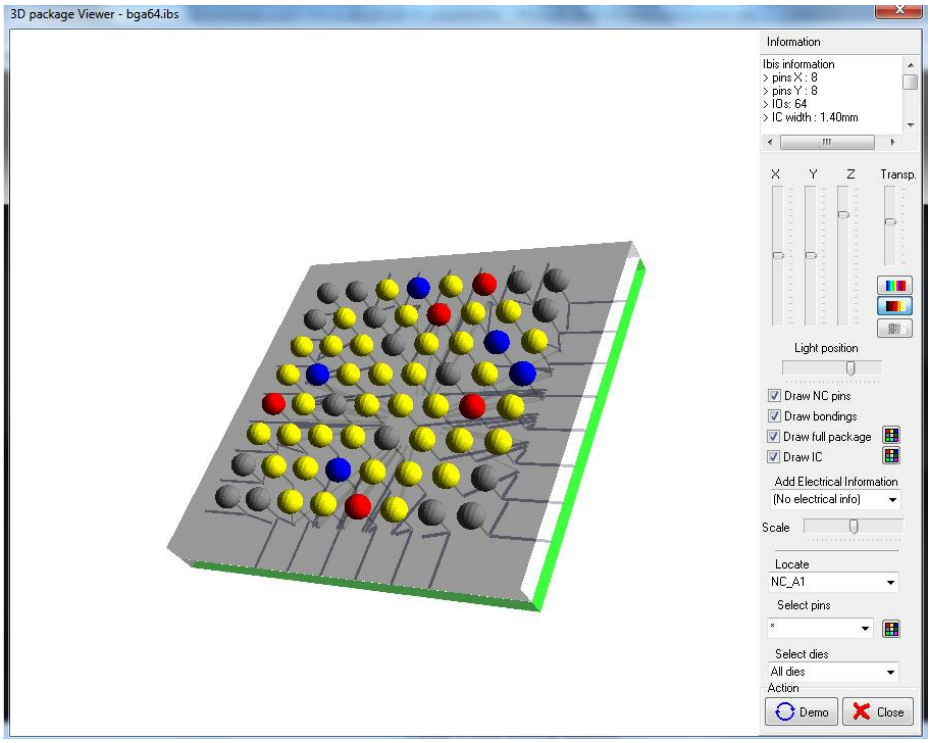


Figure 4- 36: the 3D-package viewer (examples\ibis\bga64.ibs)

IV.7.6 Advanced Package Model

The command "Tools > Advanced Packaged Model" opens a tool that generates automatically realistic model of package and compute electrical parasitic elements (R, L, C). An example is provided in part III.9.3.2. The tool supports several types of packages:

- Dual In Line (DIL), Small Outline Package (SOP): pins placed on both opposite sides of the package. The tool builds automatically a realistic geometrical model from mechanical information.
- Quad Flat Package (QFP): pins placed on all the four side of the package. The tool builds automatically a realistic geometrical model from mechanical information.
- Ball Grid Array (BGA): this type of package is quite complex because the internal redistribution tracks can be placed on several layer. Thus, an automatic geometrical model is not possible. IC-EMC proposes a 3D interface to build the geometrical model, starting from mechanical information.

The interface is composed of three tabs:

- Package generation: the first interface dedicated to the generation or the import of the geometric model of the package. Several mechanical information are required to produce the package model. Appendix H gives details of geometrical parameters. A *.geo file is generated at the end of the package definition, when the button "Generate Geo Model" is clicked. This file contains the geometrical information. If the *.geo file already exists, this file can be directly imported by clicking the button "Import Geo Model". When this tool is opened, only this tab is visible. The two other tabs become visible when a new *.geo has been generated or when a valid *.geo has been imported. Figure 4- 37 presents the first tab dedicated to package model definition.

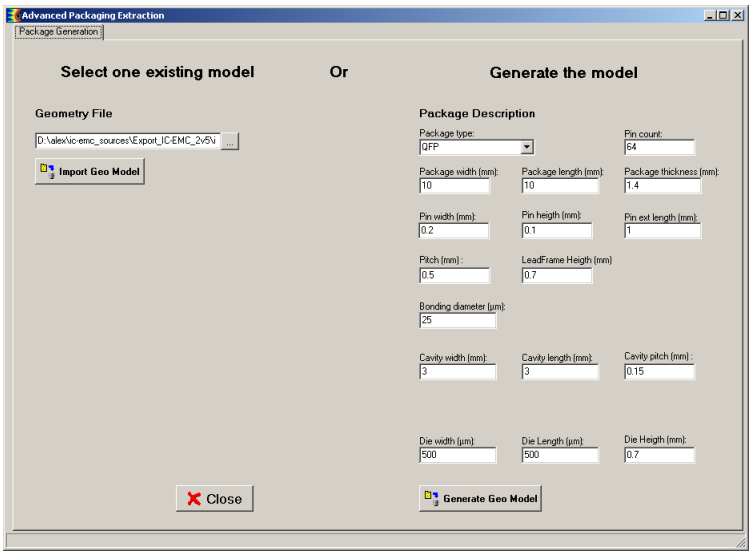


Figure 4- 37: Definition of package model, generation of .geo file

- Model viewer: after a *.geo file has been generated or imported, this tab appears to view a 3D picture of the reconstructed package, as shown on Figure 4- 38.
- Compute parasitics: this tab is dedicated to the extraction of parasitic resistance, inductance and capacitor of each individual pin of the package. The computation of electrical elements is based on a geometry meshing and a PEEC method. More details can be found in appendix H. Figure 4- 39 details the computation interface. First, configure the electrical parameter of the computation: dielectric constant, perfect ground plane presence, frequency, conductivity. Then, select the electrical parameters that you want to extract and finally click on the button “Click” to launch the computation. The simulation duration depends on the size of the package and the number of pins. Resistance extraction is very fast, while inductance and capacitor extraction take a longer time. A progression bar indicates the status of the simulation. At the end of the simulation, you can display the simulation results on the screen on the right. Simulation results for a package model saved as GEOname.geo are automatically exported in files called GEOname.R, GEOname.L or GEOname.C for resistor, inductor or capacitor extraction respectively.

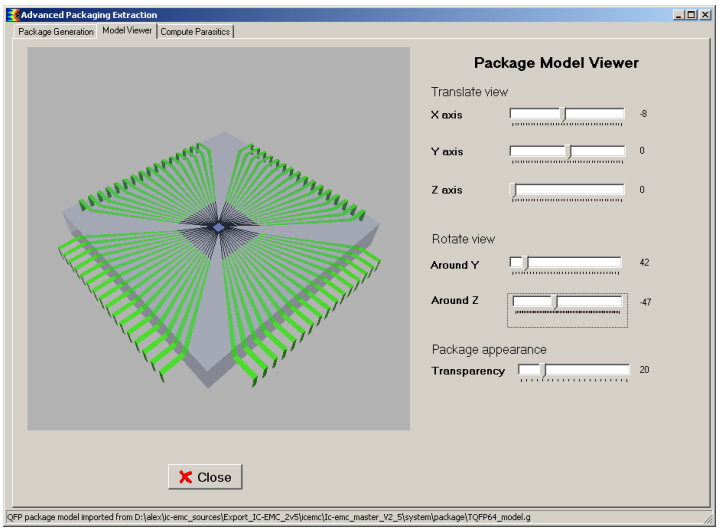


Figure 4- 38: 3D view of the advanced package (examples\package\TQFP64.geo)

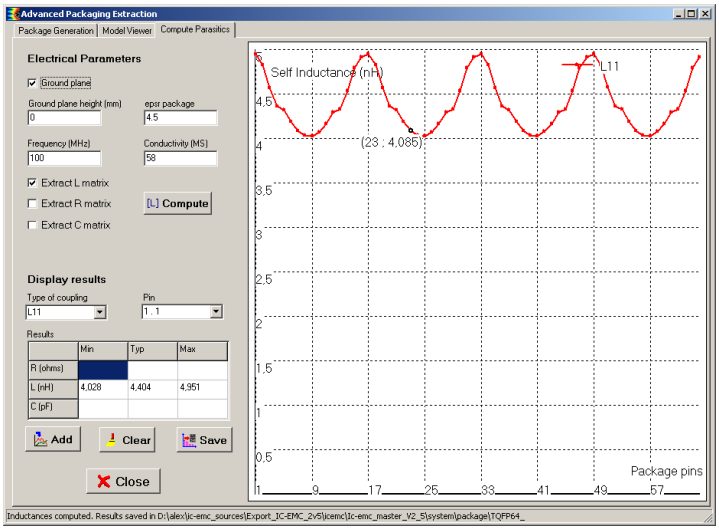


Figure 4- 39: Interface for computation and display of package electrical parasitics (examples\package\TQFP64.geo)

BGA packages are quite complex and the generation of this package type cannot be built automatically. Therefore, when the user click on the button “Generate .geo Model” after selecting “BGA“ in the field Package Type and typing package mechanical information, a special interface is opened to help user to build a custom geometrical model of a BGA package.

IV.7.7 Interconnect Parameters

The "Tools > Interconnect parameters" tool included in the Tool menu computes the R,L,C parameters of an interconnect based on its physical dimensions. Analytical formulations are used for these evaluations. An example is proposed in III.9.1.

First, select the interconnect types by choosing the adequate cross section. Enter the information about geometry and materials of the interconnect. Table 4- 5 lists the supported line sections. Then, click on “Line Model y=f(x)” to apply analytical formulations to compute the different electrical parameters of the interconnect (resistance, capacitance, inductance

per unit length, characteristic impedance, skin effect, propagation delay, loss). The computed parameters can be saved in a .txt file by clicking on the button “Save Param.”.

The right of the screen offers a tool to analyze the influence of a geometrical dimension (e.g. width of a microstrip line, thickness of substrate, etc...), material property (e.g. dielectric permittivity, conductivity, etc...) or frequency on a computed electrical parameter of the interconnect. Select the influent parameter in the list “In parameter”, its minimum and maximum value, the sweeping options (linear or logarithm sweep, number of points), the electrical characteristics to observe (list “Out parameter”) and click on the button “Plot” to plot the evolution of the Out parameter vs. the In parameter.

Finally, an equivalent SPICE model of the interconnect made of RLC cells can be automatically built. A frequency-dependent model of the losses can be included in the model by selecting the option “Include losses”. Enter the limit frequency of validity of the model (field “Freq (GHz)”) and click on the button “SPICE Model”. Automatically, if the option “Create subcircuit” is not selected, the equivalent SPICE schematic is displayed on the main screen of IC-EMC. If the option “Create subcircuit” is selected, the line model is saved in a user symbol (.sym) which can be placed on the schematic later with the command “Insert > User symbol (.SYM)”, as described in part I.4.1. You can also give geometrical coordinates to inductances of interconnects to perform near field emission simulations, by selecting the option “Near field analysis”.

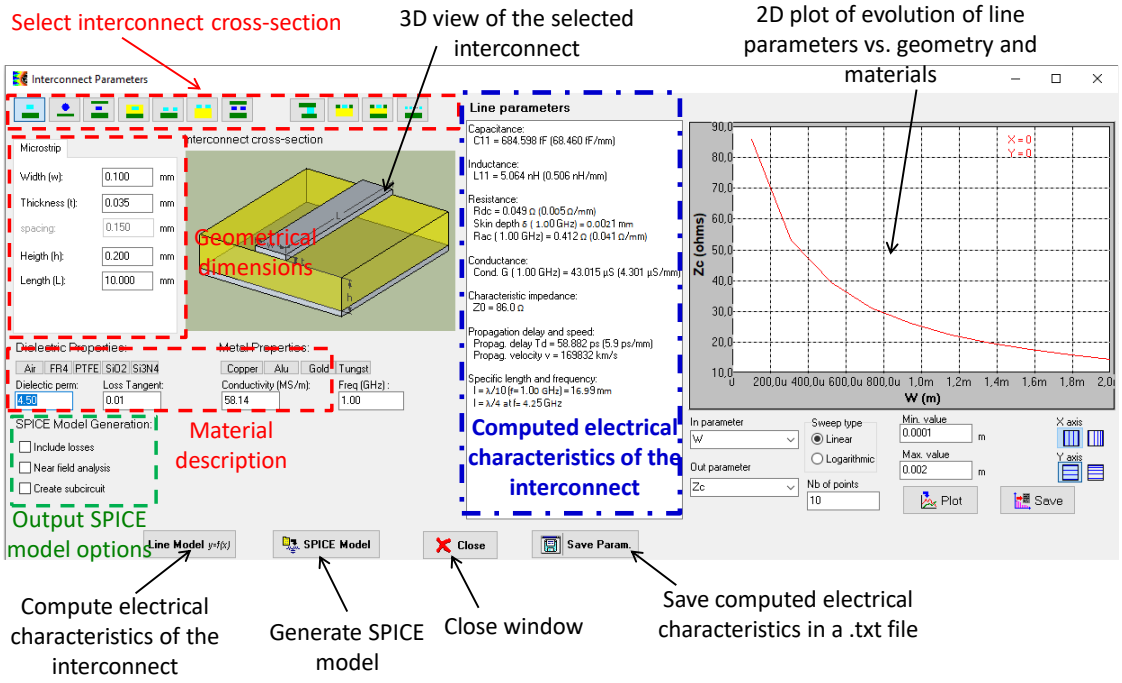


Figure 4- 40: Interconnect R,L,C model based on physical dimensions

	Microstrip line		Edge-coupled stripline
	Circular wire above ground plane		Via
	Centered stripline		Coplanar waveguide
	Burried microstrip line		Coplanar waveguide above ground plane

	Edge-coupled microstrip line		N parallel traces (N ≤ 8)
	Coplanar stripline		

Table 4- 5: Icons of cross-sections modeled in "Tools > Interconnect Parameters"

IV.7.8 Cable modeling

The command “Tools > Cable modeling” opens a screen dedicated to the modeling of basic cable cross-section (bifilar cable, wire above a ground plane, coaxial cable, shielded pair). An example is provided in III.9.2.

The principle of this tool is similar to the Interconnect Parameter tool (see part I.7.7).

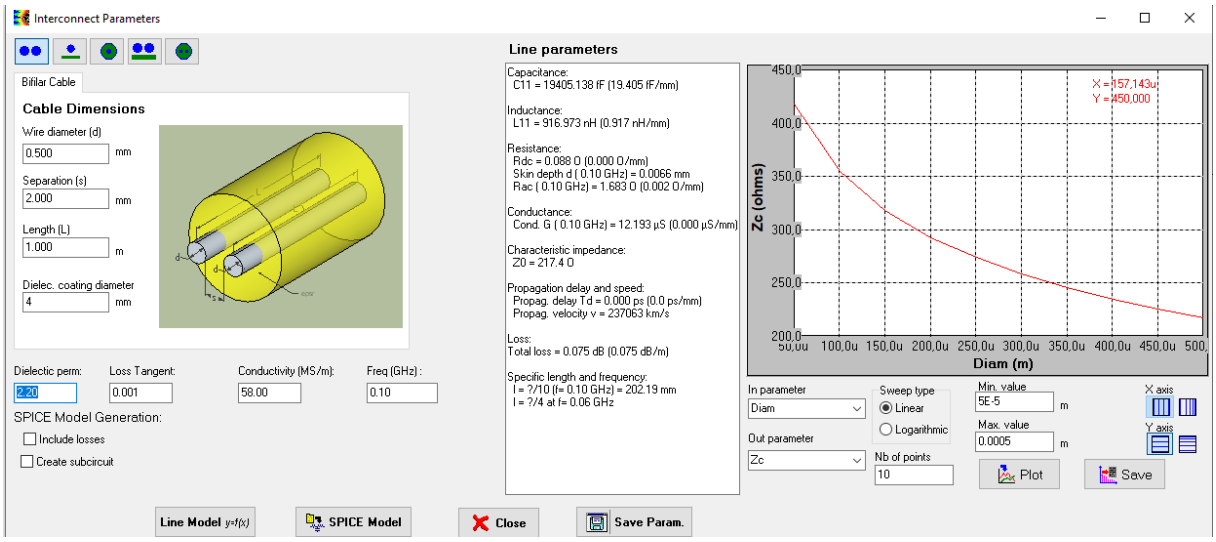


Figure 4- 41: The attenuation in cable evaluation interface

IV.7.9 PG Plane Model

The tool “Tools > PG Plane Model” is dedicated to the simulation of S or Z matrix between several ports placed on a rectangular cavity formed by a power and ground plane pair. The model relies on an analytical cavity resonator model (refer to example shown in III.9.4 for more details). The analytical method is based on the solution of Helmholtz equation with the Green’s function for rectangular plane. Figure 4- 42 presents the default screen dedicated for power and ground planes dimension and property configuration. The power and ground planes lies on (x,y) plane and are separated by the distance “Thickness”. In the table Access Point, the (x,y) coordinates of the input ports are defined. The port shape is assumed square and their width is given in the column “W (mm)”. Click on “Add access” to add a new port, or “Remove access” to remove the last defined port. The analytical computation is configured in the screen called “Model Parameters”. The maximum cavity resonance orders and the frequency sweeping configuration are defined here. Click on the button Compute Model to launch the analytical simulation. Finally, the results can be plotted on the graph on the right part of the screen, from the tab “Results” (Figure 4- 43).

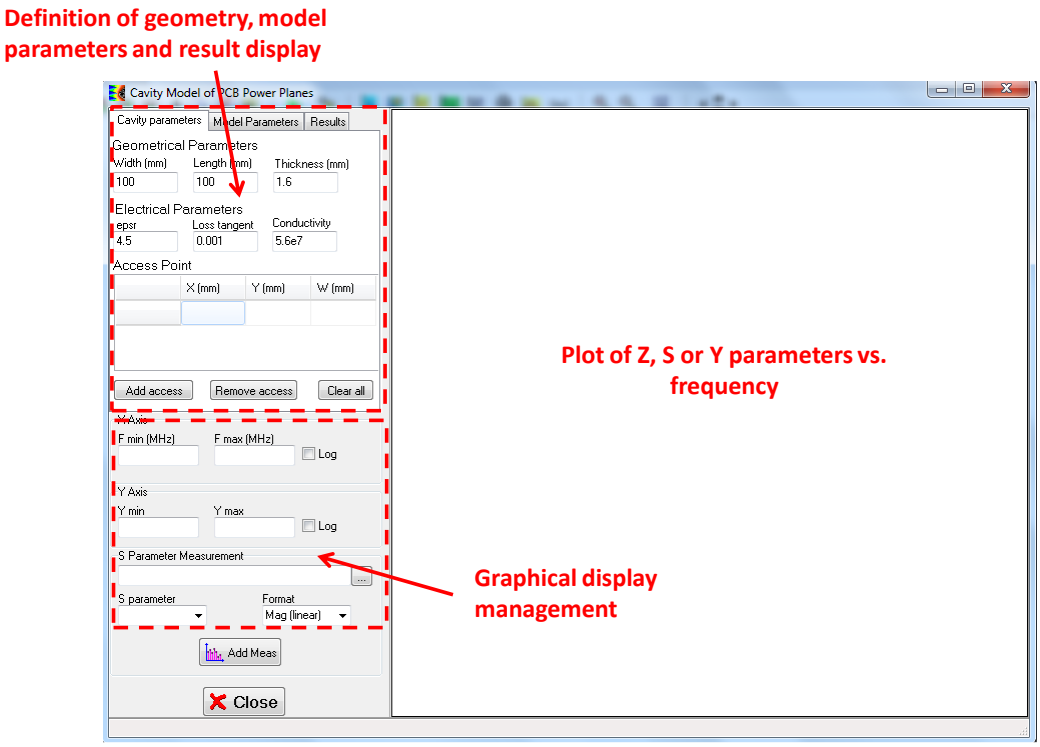


Figure 4- 42: Configuration of cavity dimensions and port placement

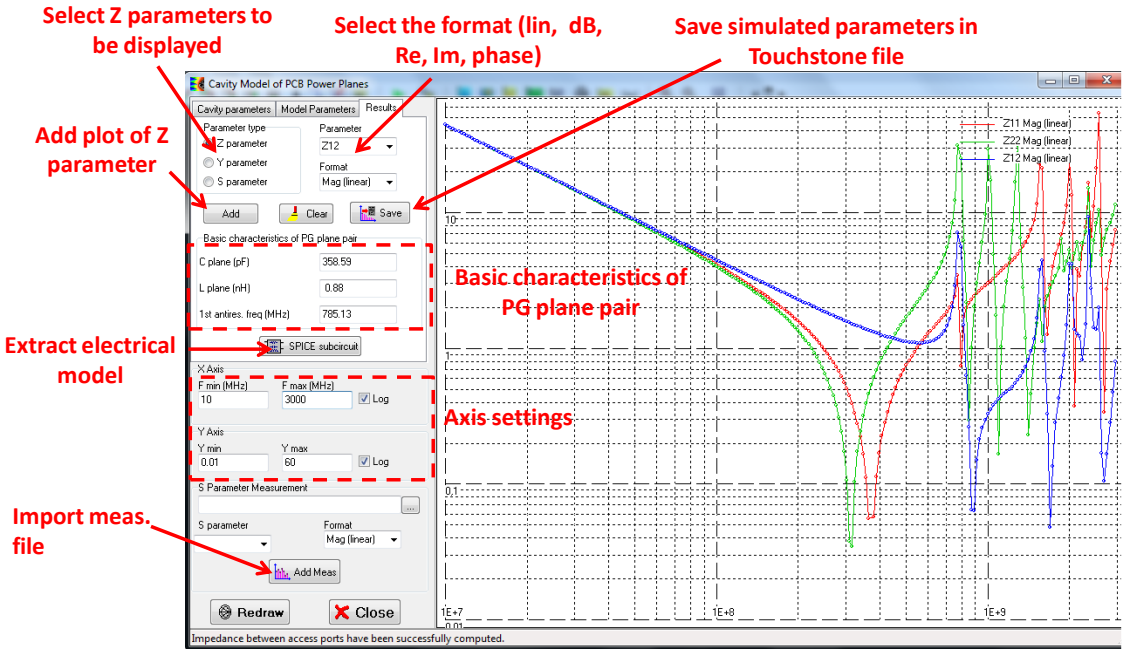


Figure 4- 43: Cavity resonator model: A result plot

The Z, S or Y parameters of the N port matrix can be plotted versus the frequency. The total inductance and capacitance of the power plane are also computed. The result can be saved in an output file in Touchstone format (*.sNp).

IV.7.10 S parameter de-embedding

The command "Tools > S Parameter Deembedding" gives access to a specific screen for deembedding a S11 parameter measurement. Deembedding a S11 parameter measurement means removing the influence of parasitic attachments (coaxial cables, microstrip lines …) used to connect the device under test input to the calibration plane of a vector network analyzer. The raw S11 measurements can be provided by a file in .s50 or Touchstone .s1p format. Data in this file can be in various formats:

- S or Z parameter
- Real and imaginary parts
- Amplitude and phase

The maximum number of frequency is limited to 4000 points. The deembedding process considers two cases:

- the DUT is connected to the calibration plane of the VNA by a perfectly matched transmission line. Only the delay T_D and thus the phase φ introduced by the line are compensated by the deembedding process, based on the following equations.

$$S_{11deemb} = \frac{S_{11meas}}{\exp(-j2\varphi)} \qquad \textit{Eq. 4- 1}$$

$$\varphi = \frac{2\pi L}{\lambda} = \frac{2\pi L f\sqrt{\varepsilon_r}}{c} = 2\pi f T_D \qquad \textit{Eq. 4- 2}$$

where

S_{11meas}: raw S_{11} measurement

$S_{11deemb}$: deembedded S11 measurement

L: the length of the feed line

T_D: time duration induced by the line

εr: the dielectric constant

f: frequency

- the DUT is connected to the calibration plane of the VNA by an unmatched 2-port attachment line (Figure 4- 44). A touchstone file .s2p must be provided by the user to characterize this device. The .s2p file of the 2-port device must contain the same number of frequency points than the raw S11 measurement file to perform the deembedding. If the frequencies in both files are not identical, validity of deembedding results cannot be ensured.

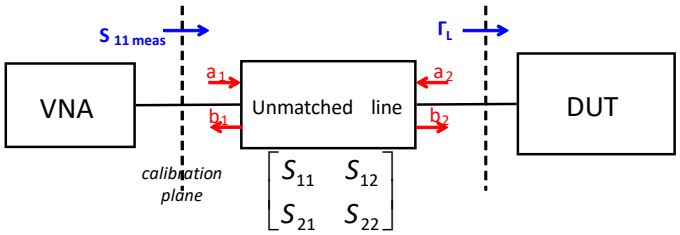


Figure 4- 44: The DUT input is connected to the VNA by a unmatched line fully characterized

Equations 4-3 and 4-4 detail the relation between S_{11meas} and the DUT input reflection coefficient Γ_L.

$$S_{11meas} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12} \times S_{21} \times \Gamma_L}{1 - S_{22} \times \Gamma_L} \quad \textit{Eq. 4- 3}$$

$$\Gamma_L = \frac{S_{11meas} - S_{11}}{S_{12} \times S_{21} + S_{22} \times \left(S_{11meas} - S_{11}\right)} \quad \textit{Eq. 4- 4}$$

The interface proposes a screen used to display the S11 raw measurement file and the deembedded results, as shown in Figure 4- 45. Data are displayed in impedance amplitude versus frequency. Deembedded results, i.e. the S11 parameter of the load after removing the parasitic attachments, can be saved in an output file in three different formats: .z, .s50 or .s1p. The two first formats are dedicated to display the results in the tool “Impedance vs. Frequency”, while the last format is dedicated to display the results in the tool “S parameters vs. Frequency”. The result can be displayed in these screens as measurements.

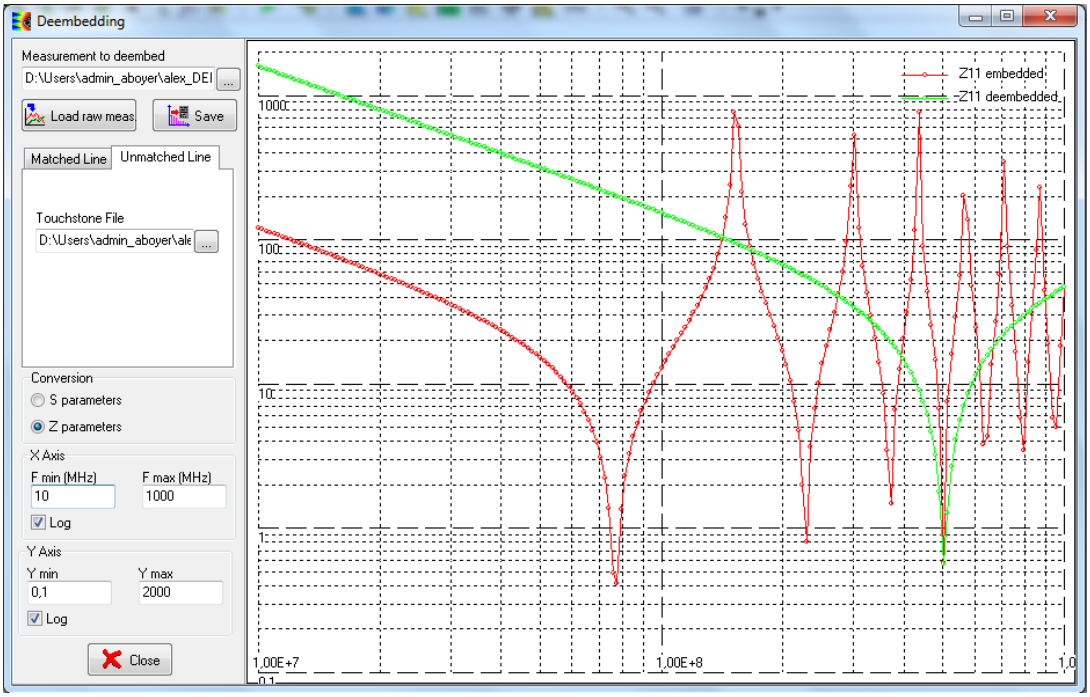
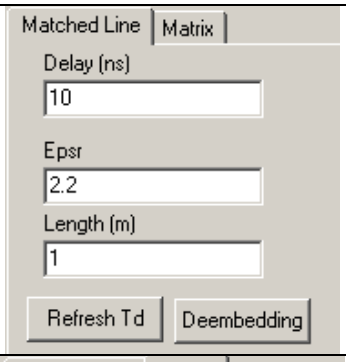
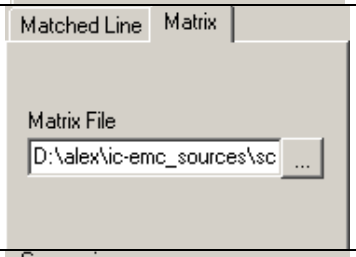
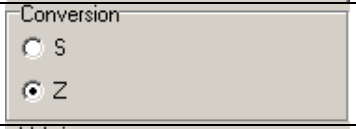
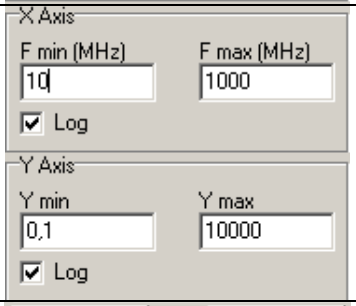


Figure 4- 45: S parameter deembedding user’s interface (examples\basic\deembed\S11_rawDeembed.s1p)

IV.7.10.1 Control Buttons

Buttons	Description
Measurement to deembed D:\alex\ic-emc_sourc ... Load	Import the S11 raw measurement file, that consists of the measurement of the device under test connected to the VNA through a matched or unmatched connection. The file could be in .s50 or .s1p format. Select the file and click on the button “Load” to load the raw measurement file and display the measurement in an impedance vs. frequency chart.

	The connection between the load and the VNA is a matched transmission line (Tab “Matched Line”). Specify the delay introduced by this line: type directly the delay in ns, or type the length and the relative dielectric constant of the line and click on the button “Refresh Td”. Once the delay has been specified, click on the button “Deembedding”. The effect of the connection is removed and the impedance profile of the extracted load is traced.
	The connection between the load and the VNA is an unmatched 2-port transmission line (Tab “Matrix”). Specify the path of the Touchstone file *.s2p which characterizes the unmatched line. Once this file has been identified, the deembedding is automatically performed. The effect of the connection is removed and the impedance profile of the extracted load is traced.
	The raw measurement and the deembeding results displayed on the screen are automatically converted in S or Z parameters when the corresponding box is selected.
	Axis settings. Each time a new curve is added, the axis settings are lost and replaced by default axis settings. The default settings are computed to display all the curves.
	Click on the button “Save” to export the deembedding results in either a .z, .s50 or .s1p file. Click “Close” to close the interface.

IV.7.11 Spectrogram

The command “Tools > Spectrogram” gives access to the display of the short-term FFT (SFFT) or spectrogram of the signal. The energy (using a palette of colors) is displayed both versus time (X axis) and frequency (Y axis). The spectrogram is obtained by computing several FFT and shifting the FFT window until the whole signal is covered, as explained in Figure 4- 46. The FFT is applied iteratively on a reduced number of points N_{FFT}, and then shifted and X and Y axis may be modified using the icons situated on the top-left corner of the screen. The spectrogram is characterized by a resolution in time and frequency domains, as given by equations 4-5 and 4-6.

$$\mathrm{Reso}_T = N_{FFT} \times T_S \quad \textit{Eq. 4- 5}$$

$$\mathrm{Reso}_F = \frac{1}{\mathrm{Reso}_T} = \frac{1}{N_{FFT} \times T_S} \quad \textit{Eq. 4- 6}$$

where N_{FFT} is the number of points used for the FFT or FFT window, and Ts is the sampling period. Both equations show that a very precise resolution in both time and frequency domains cannot be obtained. Both are controlled by the number of points of the FFT and the sampling time. Only a compromise between time and frequency resolutions can be found.

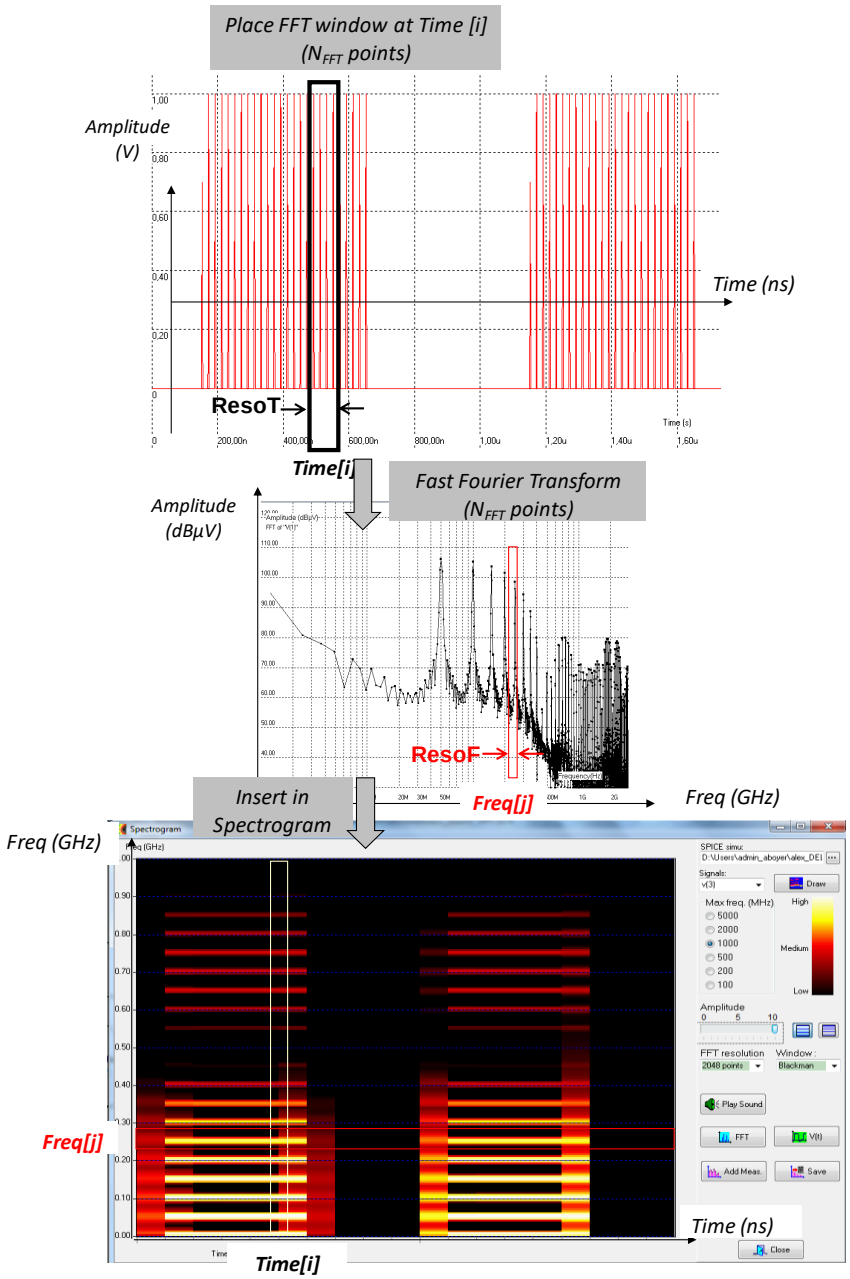


Figure 4- 46: Spectrogram principles (examples\transient\ discontinuous_source_SFFT.sch)

Figure 4- 47 describes the user's interface of the spectrogram. The input file is a SPICE transient simulation result, given by the field "SPICE Simu". Time-domain measurement in .tab format can also be downloaded by clicking on the button "Add Meas.". Then, select the signal to display (list "Signals"), select the maximum frequency for the FFT (between 100 and 5000 MHz), the number of points of the FFT window, and the windowing type (rectangular, Hamming or Blackman). Finally, click on the button "Draw" to compute the SFFT and display the spectrogram. This result can be saved in a .txt file by clicking on the button "Save".

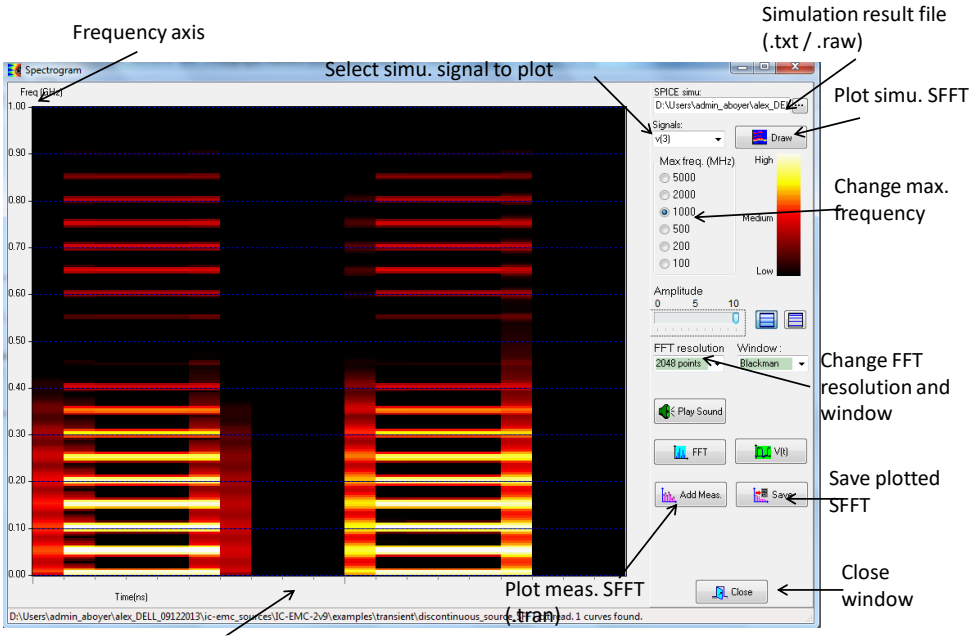


Figure 4- 47: Spectrogram user's interface (examples\transient\ discontinuous_source_SFFT.sch)

IV.7.12 Eye Diagram

The command “Tools > Eye diagram” opens a special screen for plotting eye diagram for signal integrity analysis. The tool must be launched only if a schematic containing an Eye Diagram symbol (available in the symbol palette) and the associated SPICE simulation result file exist. In these conditions, when the eye diagram tool is launched, the SPICE simulation result file name appears in the field “Simulation Data Source”. Click on the button Eye to plot the eye diagram (Figure 4- 48). The table "Signal integrity indicators" lists the average, min, max and standard deviation of several parameters which characterize signal integrity, such as eye width, eye height, rise/fall time, jitter, SNR, etc. An example is provided in part III.7.

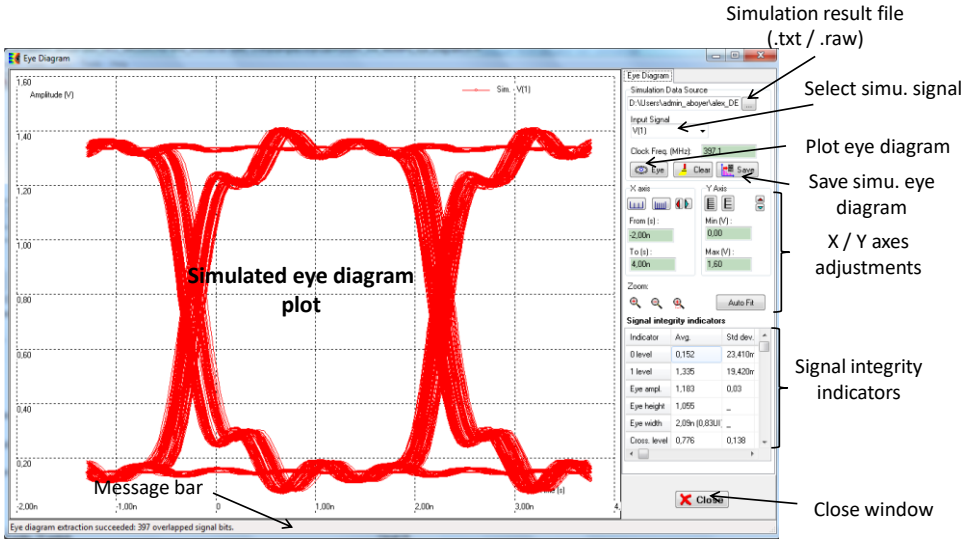


Figure 4- 48: Eye diagram plot (basic\signal_integrity\ Eye_digital_IO_switching.sch)

Remark: only one eye diagram symbol is supported by schematic. All voltage or current probes should be disabled during eye diagram simulation. Obviously, it requires transient simulation, whose duration is long enough to contain a large number of signal periods.

IV.7.13 LC Resonant Frequency

The command "Tools > LC Resonator and Filter" tool proposes a menu to analyze different electrical structures based on L-C:

- series or parallel L-C resonator (tab “Z(f) LC resonator”)
- 1st, 2nd or 3rd order EMC filter based on L-C (tab “LC filter”)

Values of inductance and capacitance are selected and the corresponding resonant frequency is calculated. When the tab “Z(f) LC resonator” is selected, the tool computes and plots the evolution of the resonator impedance according to frequency, as shown in Figure 4-49. Three L-C resonator structures can be selected:

- A series L-C resonator
- A parallel L-C resonator
- Two parallel L-C branch

A series resistance can be defined in the field “Resistor”.

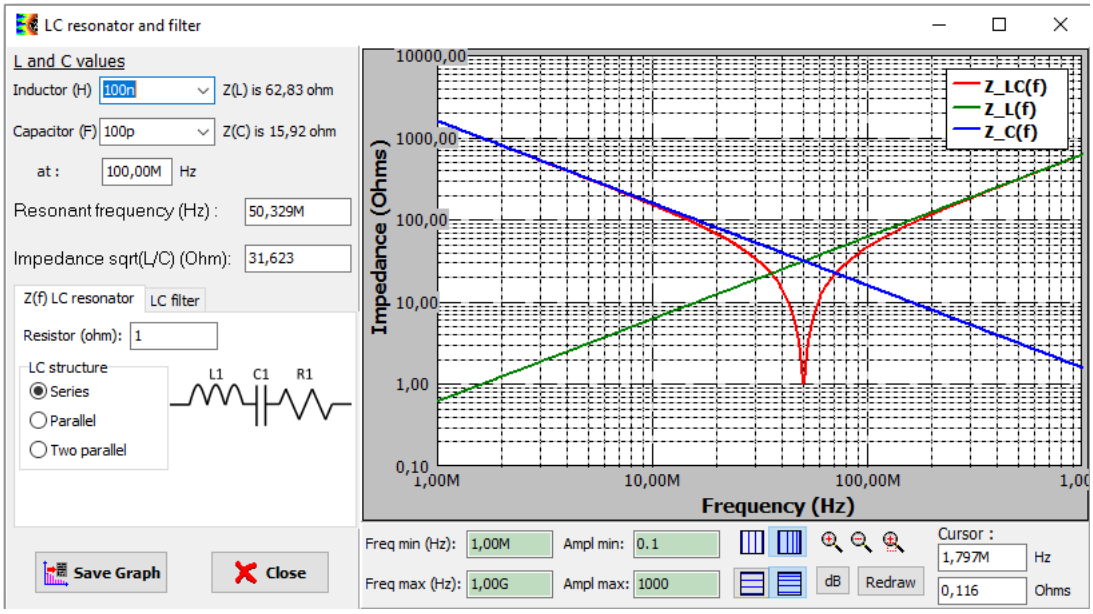


Figure 4- 49: Resonant frequency of a L-C resonator and plot of the impedance

When the tab “LC filter” is selected, the insertion of a L-C filter is plotted according to the frequency, as shown in the figure below. The structure of the filter is defined by the list LC filter type. Six configurations, based on the L and C values defined by the field “Inductor” and “Capacitor”, are proposed:

- 1st order – L: serial inductor
- 1st order – C : parallel capacitor
- 2nd order – LC

- 2nd order – CL
- 3rd order – LCL
- 3rd order - CLC

The source and output impedances are equal to 50 Ω by default, but they can be modified to the values specified in the fields “Source impedance” and “Load impedance”.

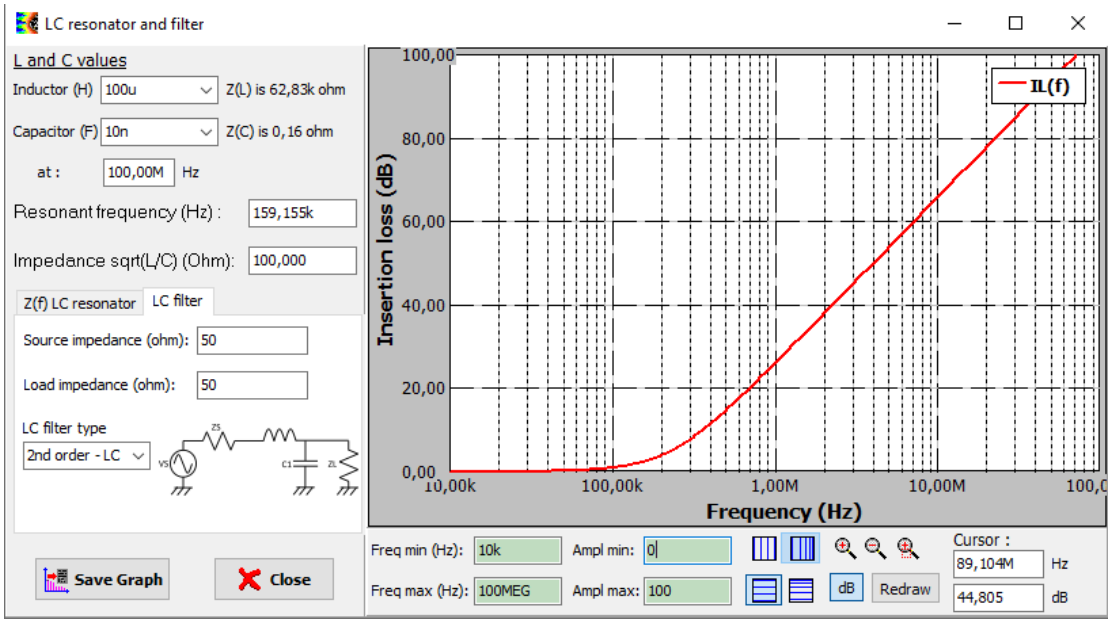


Figure 4- 50: Resonant frequency of a L-C resonator and plot of the impedance

IV.7.14 dB/Linear Unit Converter

A convenient tool has been added to the EMC menu, called “EMC unit converter”, to compute the correspondence between linear and dB units. In the example shown in Figure 4-51, the value 2V is converted into dB (6.02 dB). A value in dB may be converted into linear scale. Available units are V, A and Watts. For Watts, the log scale is 10.log(Y), and 20.log(x) for the other units.

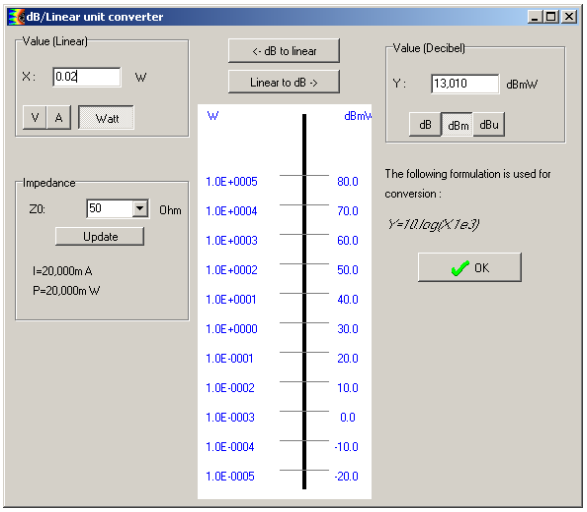


Figure 4- 51: The user’s interface for the EMC unit converter

To obtain the current, voltage or power flowing in a 50-Ohm load, click the button “Update“. In the example shown in figure 11-10, a 1.0V voltage on a 50-Ohm load results in a 20 mA current and induces 20 mW dissipation.

IV.7.15 Frequency/Wavelength Converter

The wavelength corresponding to a given frequency may be computed in a dedicated screen added to the **Tools** menu and called “**Freq./Wavelength converter**”

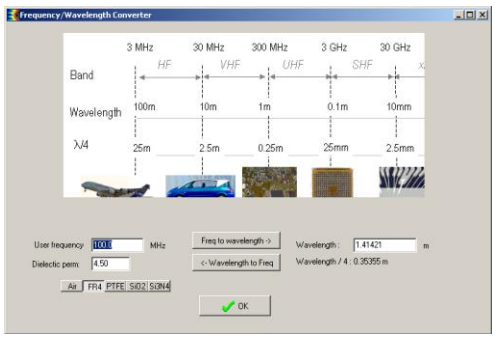


Figure 4- 52: The user’s interface for the frequency/wavelength conversion

The formulation used for conversion is as follows: $\lambda = \frac{c}{f\sqrt{\varepsilon_r}}$

Material	Relative permittivity
Air	1
FR4	4.6
PTFE	2.2
SiO2	3.9
Si3N4	7

IV.7.16 Cavity Resonant Frequency

Numerous systems can be modeled as resonant cavity from an electromagnetic point of view: box or package with metallic enclosure, power-ground plane pair in a multilayer PCB (see IV.7.9 for the particular case of rectangular power-ground plane pair). These structures can have various geometry and dimensions, but they are characterized by particular conditions at their boundaries: conductive and opened boundaries. The geometries and the boundaries force the existence of only some propagation modes of electromagnetic waves. Typically, transverse electromagnetic (TEM) waves cannot propagate within such cavity. Only transverse electric (TE) and/or transverse magnetic (TM) waves may propagate, above resonant frequencies F_{mnp} which depend on cavity's geometry, dimensions and boundary conditions. Here, the integer indices m, n and p designate one propagation mode.

From an EMC point of view, these resonant frequencies have a major practical interest, since emission and susceptibility issues may arise around these frequencies. Cavities may behave as efficient parasitic antennas and generate non negligible radiated emission or couple a significant amount of radiated incoming disturbances.

In practical applications with complex geometry, apertures, presence of cables, etc…, exact formulations of resonant frequencies are either extremely complex or impossible to derive, and numerical electromagnetic simulations are required. However, for some canonical geometrical shape, closed-form expressions may be derived to compute resonant frequencies precisely. This is the case for 2D or 3D rectangular cavity. In spite of the

simplification of the geometry, such expressions may be helpful to evaluate the range of the first resonant frequencies and identify possible EMC risks.

The 3D cavity is the general case for a rectangular cavity and 2D cavity is an approximation. 2D rectangular cavity means that one dimension (e.g. the height) is negligible compared to the wavelength, in contrary to the two other dimensions (e.g. the width and the length). The formulation for the resonant frequencies of a 3D cavity is given by equation 4-7 while equation 4-8 provides the resonant frequencies in the case of a 2D cavity.

$$F_{mnp} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2 + \left(\frac{p}{H}\right)^2} \qquad \textit{Eq. 4- 7}$$

$$F_{mn} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2} \qquad \textit{Eq. 4- 8}$$

where:

$F_{mn(p)}$=resonant frequency (Hz)

ε= permittivity = $\varepsilon_0\varepsilon_r$, ε_0= 8.85x10^{-12} F/m, ε_r= 3.8 (for SiO_2)

μ= permeability= $\mu_0\mu_r$, μ_0= 4π.10^{-7} H/m, μ_r= 1 (Air)

m, n, p =mode (integer 0,1,2..)

L=length of the rectangular cavity (m)

W=width of the rectangular cavity (m)

H=height of the rectangular cavity (m)

The screen “Tools > Cavity resonant frequency” computes the resonant frequencies of 2D or 3D resonant cavity according to the previous formulation. Figure 4- 53 describes the tool. Select 2D or 3D cavity model, set the cavity dimensions, the dielectric permittivity of the cavity medium. Finally, click on the button "Generate Freqs" to compute the resonant frequencies for propagation mode indices m, n, p from 0 to 9. The resonant frequencies are summarized in the table "Resonant frequencies" according to m and n indices. The table is given only for one p index. The computed resonant frequencies can be saved in a text file by clicking on the button "Save".

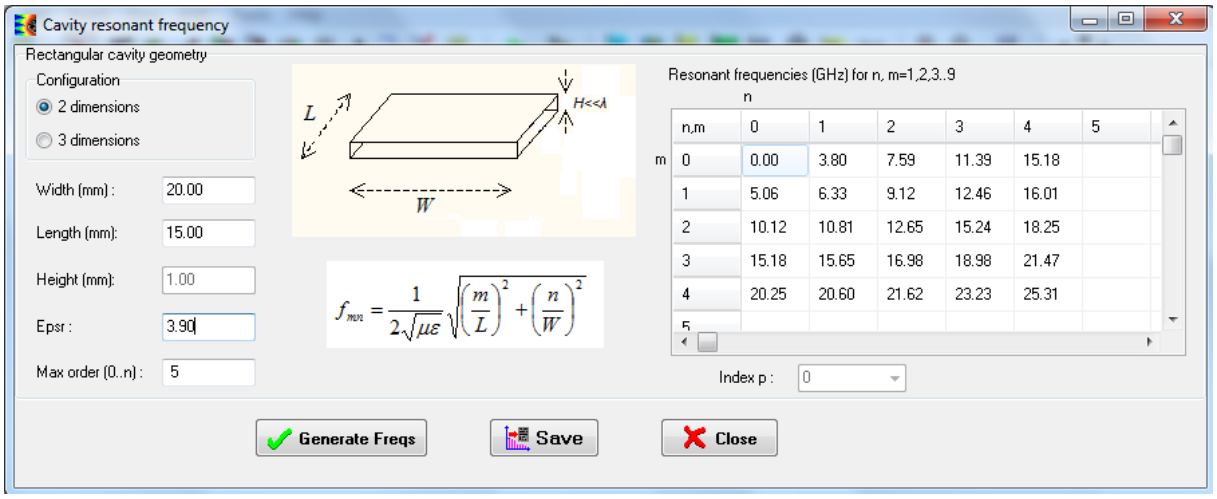


Figure 4- 53: Computation of the resonant frequencies of a rectangular 2D/3D cavity

IV.7.17 Intermodulation products

When non linear devices are excited by several signals, the distortion of these signals induced by the device behavior leads to new harmonic content due to intermodulation products. The command “Tools > Intermodulation products” offers a simple calculator of frequencies of the new harmonics produced by the intermodulation products between two harmonic excitation signals F1 and F2 (Figure 4- 54). These new harmonics are characterized by two integer numbers (m,n) related the order of the intermodulation product, such that their frequency Fmn is given by:

$$F_{m,n} = \pm m \times F_1 + \pm n \times F_2 \qquad \textit{Eq. 4- 9}$$

The frequencies of both input signal are given in MHz, the maximum order for m and n is given in the field Max. Harmonic Index”, which is limited to 100. Click on the button Compute to extract the intermodulation product frequencies. The results are displayed in two tables: The “Frequency Planning Array” (on the left) gives the intermodulation product frequency value versus (m,n) couple. The “List of Frequency” (on the right) gives a list of all the new harmonic frequencies in ascending order. Click on the button Save to write both tables in an output file *.txt.

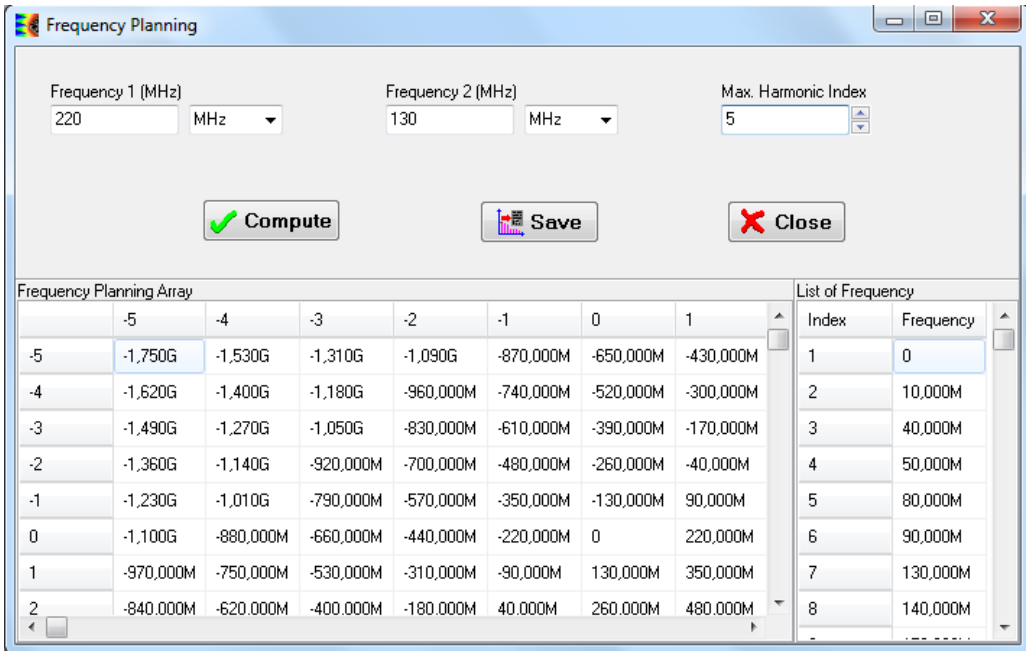


Figure 4- 54: Calculation of the frequencies of intermodulation products between 2 harmonic signals

v. Description of the symbols

Schematic diagrams are built with a set of symbols, available either in the symbol palette or in the subdirectory "IEEE" of the installation directory of IC-EMC. Symbols are saved in .sym files and have a double purpose:

- graphical symbol of a component instance, simulation command or schematic illustration
- definition of the parameters of a component instance

In this part, the different symbols proposed by IC-EMC are listed.

V.1 Components of the Symbol Palette

The most common schematic symbols are reported in the Symbol Palette, which is visible by default on the right part of the main screen of IC-EMC. This palette can be closed and reopened with the command "View > Symbol Palette". Figure 5- 1 shows the Symbol Palette. Table 5- 1 describes each symbol of the Symbol Palette. The name of the symbol (.sym file) is also given. All the .sym files can be found in the ieee subdirectory, within the IC-EMC main folder.

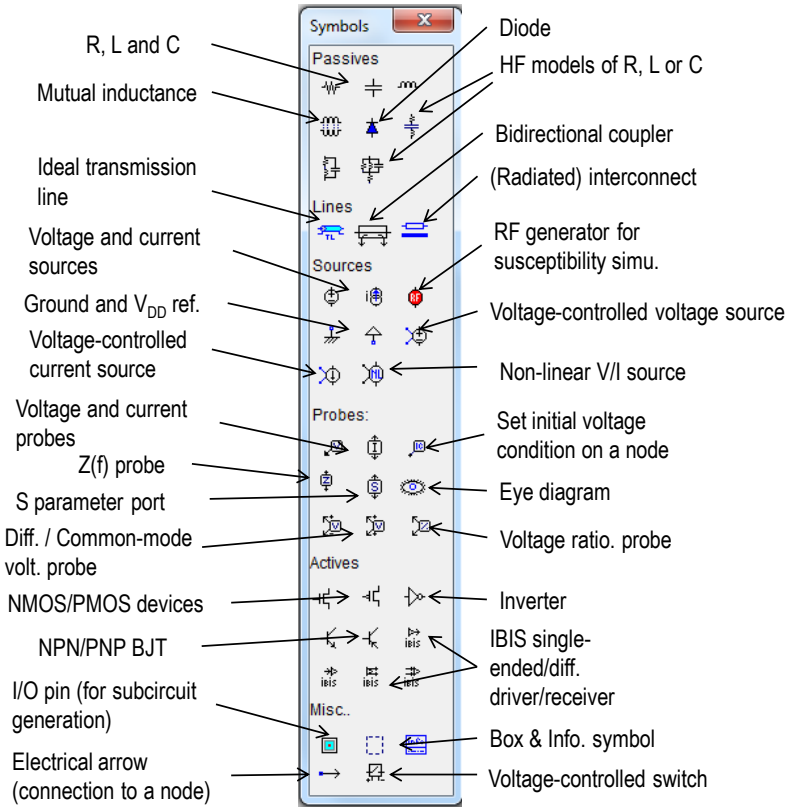


Figure 5- 1: Symbol Palette

Element	Description	Symbol name
Resistor	Resistor between two nodes	res.sym
Capacitor	Capacitor between two nodes	capa.sym
Inductance	Inductance between two nodes. With the “Assign [x;y] coordinates” property, “radiating inductance” can be defined for H field simulation (Near field scan simulation).	self.sym
Diode	PN junction or diode device. Use “spice.lib” (default library) or any other user-defined library where the diode parameters can be described and modified.	Diode.sym
Mutual Coupling	Defines the mutual coupling between two inductances.	mutual.sym
Chf	Basic high frequency model of a capacitor	Chf.sym
Rhf	Basic high frequency model of a resistor	Rhf.sym
Lhf	Basic high frequency model of an inductor	Lhf.sym
Radiated interconnect	Interconnect defined by a lumped pi-RLC cell. (X;Y;Z) coordinates, width and length are attributed to the interconnect. The property “Allow near field scan computation” ensures the simulation of E and H field (Near field scan simulation).	Interco.sym
T-Line	Transmission line, with user-accessible T0, Z0, or delay parameters	tline.sym
Coupler	Bidirectional coupler, required to extract forward and reflected voltage or power (on 50 Ω load). This element must be inserted during susceptibility simulation.	Coupler.sym
V-source	Voltage source	vsource.sym
I-source	Current source	isource.sym
RFI-source	Radio Frequency interference source, used for immunity simulations. Includes a programmable frequency generator with linearly increased amplitude vs time.). This element must be inserted during susceptibility simulation.	rfi.sym
Ground	Ground connection equal to 0.0V	vss.sym
Supply	Supply source with DC value equal to the default supply value that is found in the technology configuration file “default.tec”	vdd.sym
Voltage controlled voltage source	Linear voltage controlled voltage source. This source can model an ideal amplifier with a constant voltage gain.	vcvs.sym
Voltage controlled current source	Linear voltage controlled current source. This source can model an ideal amplifier with a constant transconductance.	vcis.sym
Non linear source	Non linear voltage or current source, called B element in WinSPICE syntax.	Belement.sym
V-probe	Voltage probe (voltage measured according to the potential 0)	probe.sym
I-probe	Current probe (serial probe with orientation marked by + symbol).	probeI.sym
IC	Initial conditions. Used to fix the start value of a node (V).	ic.sym
Z-probe	Used to generate an AC sinusoidal source to extract the impedance vs. frequency	probez.sym
S-probe	Used to declare port for S parameter analysis.	Sport.sym
Eye diagram probe	Eye diagram probe is required to plot an eye diagram. Only one active eye diagram probe should be placed on the schematic. Eye diagram plot requires a transient simulation.	EyeDiag.sym
V diff-probe	Differential-mode voltage probe (voltage difference measured between two nodes)	probeVdiff.sym
V cm-probe	Common-mode voltage probe (average voltage measured	probeVcm.sym

	between two nodes)	
Voltage ratio probe	The symbol computes the ratio between the voltages applied on its both terminals. It is useful to compute transfer function or insertion loss.	probeVratio.sym
nMOS device	N-channel MOS device. The symbol shows three terminals: gate, drain and source. Use “spice.lib” (default library) or any other user-defined library where the MOS parameters can be described and modified.	nmos.sym
pMOS device	P-channel MOS device. The symbol shows three terminals: gate, drain and source. Use “spice.lib” (default library) or any other user-defined library where the MOS parameters can be described and modified.	pmos.sym
CMOS inverter	Inverter that combines one nMOS as pull down and one pMOS as pull-up. Use “spice.lib” (default library) or any other user-defined library where the MOS parameters can be described and modified.	inv.sym
NPN BJT	NPN bipolar junction transistor. Use “spice.lib” (default library) or any other user-defined library where the BJT parameters can be described and modified.	npn.sym
PNP BJT	PNP bipolar junction transistor. Use “spice.lib” (default library) or any other user-defined library where the BJT parameters can be described and modified.	pnp.sym
Output buffer	Single-ended output buffer instance. The model of the buffer is derived from IBIS and is given by a .sym file.	BufferOut.sym
Input buffer	Single-ended input buffer instance. The model of the buffer is derived from IBIS and is given by a .sym file.	BufferIn.sym
Diff. output buffer	Differential output buffer instance. The model of the buffer is derived from IBIS and is given by a .sym file.	BufferDiffOut.sym
Diff. input buffer	Differential buffer instance. The model of the buffer is derived from IBIS and is given by a .sym file.	BufferDiffIn.sym
I/O	Input/output symbol. Used to specify the name of the I/O of a sub-circuit, during the sub-circuit definition process	io.sym
Box	Size-programmable dotted box	box.sym
Information	Information symbol with fields such as: author, date, file, project, or comments	info.sym
Arrow	Define an electrical connections between wires connected to arrow with the same name (the name of the arrow is arbitrary).	Arrow.sym
switch	Voltage controlled source. Use “spice.lib” (default library) or any other user-defined library where the switch parameters can be described and modified.	switch.sym

Table 5- 1: Description of the symbol of the palette

V.2 Components in the subdirectory ieee

Additional symbols may be found in the “ieee” subdirectory, accessible through the command "Insert > User Symbol".

Element	**Description**	**Symbol name**
AND gate	Ideal AND gate	AND.sym
Op. amplifier	Ideal operational amplifier, with configurable gain	aop.sym

Dig. oscilloscope	Digital oscilloscope for voltage probing. The sampling and the cut-off frequencies are configurable.	DigOscillo.sym
Zener diode	Zener diode. Use “spice.lib” (default library) or any other user-defined library where the diode parameters can be described and modified.	diodeZ.sym
D latch	Ideal D latch	Dlatch.sym
NOT gate	Ideal NOT gate	NOT.sym
NAND gate	Ideal NAND gate	NAND.sym
NOR gate	Ideal NOR gate	NOR.sym
4-term. nMOS	4 terminal N-channel MOS device. The symbol shows four terminals: gate, drain, source and substrate. Use “spice.lib” (default library) or any other user-defined library where the MOS parameters can be described and modified.	nmos4.sym
Alpha NMOS	Alpha-power or Sakurai model NMOS device	nmosA.sym
OR gate	Ideal OR gate	OR.sym
Pad	Graphical symbol for an I/O pad	Pad.sym
PadIn	Graphical symbol for an input pad	Padin.sym
PadOut	Graphical symbol for an output pad	PadOut.sym
4-term. pMOS	4 terminal P-channel MOS device. The symbol shows four terminals: gate, drain, source and substrate. Use “spice.lib” (default library) or any other user-defined library where the MOS parameters can be described and modified.	pmos4.sym
Alpha PMOS	Alpha-power or Sakurai model NMOS device	pmosA.sym
Schmitt trigger	Ideal Schmitt trigger.	SchmittBuff5V.sym
Coax. connector	Graphical symbol for a coaxial connector (e.g SMA connector)	Sma.sym
TDR	TDR generator (Time Domain Reflectometry). The pulse voltage, rise time and width are configurable, as the output voltage.	TDR.sym
XOR gate	Ideal XOR gate	XOR.sym
XNOR gate	Ideal XNOR gate	XNOR.sym

Table 5- 2: Description of the additional symbol accessible in the subdirectory ieee

VI. Input/output file format

VI.1 TAB File Format

The TAB file format is generated by several equipments, and corresponds to a text document, organized with the frequency (Hz) in the first column, followed by spectrum energy in the remaining columns (dBµV, V, dBµA, etc…). The heading of the file is made of comment lines which are ignored during the reading of this file, except the line which indicates the nature of the column of data. This line must start with the special symbol '|'. In this line, units must be specified after the name of the column and must be in brackets. The first column is the frequency.

This is the most common exchange file for emission and susceptibility measurement. This file can be easily produced from measurement files generated by measurement equipment.

```
Comment Line 1
Comment Line 2 ...
|Frequency (Hz) Voltage (dBuV)
10E6                  2.11656
10.05E6         -1.02154
10.1E6          -4.87756
…
```

VI.2 Z Format

The Z file is similar to the .tab file, except that it is dedicated to import/export the measurement of impedance magnitude done on a single port. This file consists of the frequency followed by the module of the impedance. . The heading of the file is made of three comment lines which are ignored during the reading of this file.

```
CAPA  Impedance
100pF A5 impedance vs frequency
Freq(Hz) Z(f)
45000000  25.96613733
57443750  15.90372125
69887500  10.70620745
82331250  7.724689023
94775000  5.852317536
…
```

VI.3 Touchstone file – SnP

Touchstone files *.snp" [TOU02] are standard ASCII text file used to exchange measurement done with vector network analyzer on an n-port device, such as S, Z, Y… parameters or noise measurement. the index "n" gives the number of ports used for the measurement. IC-EMC can import and export S parameter measurement and simulation results up to 4 ports, so that only .s1p to .s4p files can be imported or exported. .S1P file is read by the "Impedance vs. frequency tool" which is dedicated to the plot of the impedance of one-port device. The tool "S parameters analysis" is the general tool to plot impedance and S

parameters from one up to four ports. .S1p and .s2p files are also read by the tool "S parameter Deembedding".

In order to identify the type and the format of data exported by the Touchstone file, the heading of the file includes an option line which starts by a '#' symbol. Lines which begin by a '!' are comment lines, the other are associated to data. For s1p and s2p files, all the lines start with the frequency followed by the data at this particular frequency. The general format of the option line is:

<frequency unit> <parameter> <format> R <n>

- Frequency unit: specifies the frequency unit. GHz, MHz, KHz, Hz, the default value is GHz.
- Parameter: specifies the type of network parameter data contained in the file. S for scattering parameters, Z for impedance parameters, Y for admittance parameters…
- Format: specifies the format of the network parameter data contained in the file: MA for magnitude in linear + angle, DB for magnitude in dB + angle, RI for real + imaginary. Angles are always given in degree.
- R n: specifies the reference resistance in ohms. By default, the resistance n is 50 ohms.

The following paragraph presents an example of Touchstone file for a 2 port device S parameter characterization.

```
! FILE NAME
! DATE 04/16/2005  11:30
! CORRECTED   DATA
# GHz    S       MA      R    50.00
!   FREQ       S11M         S11A     S21M         S21A      S12M
S12A      S22M        S22A
 0.040000000 1.005455E+00   -4.544 1.851869E-03 -125.819 3.100761E-03
92.047 9.720316E-01  -48.382
 0.046225000 1.004641E+00   -5.303 9.987922E-04  150.437 1.392118E-03 -
129.477 9.695778E-01  -84.433
 0.052450000 1.000527E+00   -6.231 3.931841E-04 -114.647 4.805698E-04 -
157.052 9.653241E-01 -120.483
```

The organization of .s3p and .s4p is less trivial. The file heading is the same than .s1p or .s2p files. However, for each frequencies, the parameters are arranged in a matrix format. The example below describes the organization of a .s3p file. The organization of a .s4p file is similar, except the matrix is 4x4.

```
! FILE NAME
! DATE 04/16/2005  11:30
! CORRECTED   DATA
# GHz    S       MA      R    50.00
!freq magS11 phS11 magS21 phS21 magS31 phS31 magS12 phS12 magS22 phS22
magS32 phS32 magS13 phS13 magS23 phS23 magS33 phS33
1000000 0,374992 -0,1109908 0,002356106 89,46899 0,624989 -0,1709924
0,002356106 89,46899 0,9999655 -0,3599879 0,003926845 89,505
0,624989 -0,1709924 0,003926845 89,505 0,374987 -0,3749878
```

In the “Impedance vs. frequency” interface, the conversion between Z11 and S11 parameters is given by the following equations:

$$S_{11} = S_{11\_\mathrm{Re}} + jS_{11\_\mathrm{Im}} = S_{11\_mag}\exp\left(-j.S_{11\_ph}\right) \qquad \textit{Eq. 6- 1}$$

$$Z_{11} = Z_{11\_\mathrm{Re}} + jZ_{11\_\mathrm{Im}} = Z_{11\_mag}\exp\left(-j.Z_{11\_ph}\right) \qquad \textit{Eq. 6- 2}$$

$$Z_{11\_\mathrm{Re}} = Z_0\frac{1 - S_{11\_\mathrm{Re}}^2 - S_{11\_\mathrm{Im}}^2}{\left(1 - S_{11\_\mathrm{Re}}\right)^2 + S_{11\_\mathrm{Im}}^2} \qquad \textit{Eq. 6- 3}$$

$$Z_{11\_\mathrm{Im}} = Z_0\frac{2S_{11\_\mathrm{Im}}}{\left(1 - S_{11\_\mathrm{Re}}\right)^2 + S_{11\_\mathrm{Im}}^2} \qquad \textit{Eq. 6- 4}$$

where Z_0 is the reference characteristic impedance (usually 50 Ω). For the general case of multiport device (n ≥ 1), the conversion is given by the following equations, where [Z], [S] and [I] are the Z parameter, the S parameter and the identity matrices respectively.

$$[Z] = Z_0\frac{[I]+[S]}{[I]-[S]} \qquad \textit{Eq. 6- 5}$$

$$[S] = \frac{[Z]-Z_0[I]}{[Z]+Z_0[I]} \qquad \textit{Eq. 6- 6}$$

In the "S parameter analysis" window, S and Z parameters can be represented either in singled-ended mode (the usual representation mode) or in mixed-mode representation. The mixed-mode representation is convenient in problems where common-mode and differential mode characterization is necessary. Mixed-mode representation is proposed only for 2 or 4-port models or measurements. The following equation gives the relation to convert S parameter matrix from single-ended to mixed-mode representation:

$$[S_{MM}] = \begin{bmatrix} S_{DD} & S_{DC} \\ S_{CD} & S_{CC} \end{bmatrix} = [T][S][T]^{-1} \qquad \textit{Eq. 6- 7}$$

where [S] is the S parameter matrix in single-ended mode and $[S_{MM}]$ the S parameter matrix in mixed-mode. S_{DD} and S_{CC} are submatrices related to differential-mode and common-mode respectively, while S_{DC} and S_{CD} are related to differential-to-common mode conversion and common-to-differential mode conversion respectively. [T] is a transformation matrix given by:

$$[T] = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & -1 \\ 1 & 1 \end{bmatrix} \qquad \textit{Eq. 6- 8}$$

VI.4 File .tran

The .TRAN file format is generated by time-domain measurement equipments, such as oscilloscope. It corresponds to a text document, organized with the time (s) in the first column, followed by the measured voltage in the remaining column. The heading of the file is made of several comment lines which are ignored during the reading of this file, except the line which starts with the special symbol '|'. This line indicates the nature of the different columns and the units, which is written in brackets.

This is the most common exchange file for emission and susceptibility measurement. This file can be easily produced from measurement files generated by measurement equipment.

```
Comment Line 1
Comment Line 2
|Time (s) Voltage (V)...
-1.006e-07 0.00125
-9.855e-08 0.03875
-9.655e-08 0.073125
-9.455e-08 0.1075
-9.255e-08 0.1325
-9.055e-08 0.16375
…
```

VI.5 .XY format for near-field scan measurement results exchange

The .XY format is a basic text file that contains near-field scan measurement results on a rectangular XY plane and obtained at one frequency and one altitude (Z). This format is dedicated to simple import of raw measurement file.

The file contains a header made of three lines. The first two lines are not interpreted by the "Near-field scan" tool and are displayed in the "Information" tab of the tool. It is recommended to write information about the measurement conditions in this first two lines (e.g. frequency, scan altitude, measured field, type of probes, etc…). The third line provide basic information about the measurement conditions. It starts by the special symbol '|' with the following eight parameters:

```
|Number_Points_X  Number_Points_Y  StartX(m) StartY(m)  StepX(m) StepY(m)
Field_component  Frequency(Hz)
```

Number_Points_X and Number_Points_Y gives the number of points along X and Y axes that form the scan rectangular area. StartX and StartY are the initial point of the scan area. StepX and StepY define the scan steps along X and Y axes. All the geometrical coordinates are given in meter. The sixth parameter Field-component provides the nature of the measured field component (E or H field, X, Y or Z component). Finally, the last parameter provides the frequency of the measurement.

The measurement results are arranged in a XY matrix after these three lines. Each row of the matrix contains near-field measurement at a constant coordinate Y.

VI.6 XML Near-field Scan Standard implementation in IC-EMC

Near-field scan measurements and simulations generate a large amount of data. The format of the data is closely linked to the supplier of the acquisition or simulation software, rendering extremely difficult its exchange between suppliers, customers, EDA tool vendors, academics, etc. The XML format proposed in [She09] describes how a common exchange format for near-field scan data has been developed. The format caters for various coordinate systems and is suited to emission and immunity testing both in the frequency and time domains.

VI.6.1 Principles

The techniques used for NFS are constantly evolving and the universal exchange format must allow future techniques to be included without the need for complete remodeling. The format should also be portable between operating systems, as well as both human and machine readable. The XML format meets these requirements perfectly. The use of keywords allows information to be included only as required. Additional keywords can be added to cater for new techniques, although they may not be interpreted by older software versions.

The ASCII representation of XML allows the files to be created modified and merged either manually, for example with text processors, or with simple scripts. Expensive specific software is not required for managing the files.

NFS techniques are used for measuring radiated emission and radiated immunity levels. The exchange format allows for both of these cases, but not in the same document, by enclosing all the information in a root XML element whose "Scantype" keyword may be either "EmissionScan" or ImmunityScan". A simple exchange file is shown in Figure 6- 1.

```
<?xml version="1.0" encoding="UTF-8"?>
<EmissionScan>
	<Nfs_ver>1.0</Nfs_ver>
	<Filename>Minimum_NFS_file.xml</Filename>
	<File_ver>1</File_ver>
	<Data>
		<Measurement>
			<List>
26e-3 29e-3 2e-3 -58
			</List>
		</Measurement>
	</Data>
</EmissionScan>
```

Figure 6- 1: Example file for scan emission

In order to ensure portability and compressibility, only relative paths can be used to define a path name. An absolute path is not exportable. All XML files concerning the NFS project must be placed in the same directory and other files containing data, pictures, documentation, etc must be placed in the same directory or in subdirectories.

The XML file is divided into sections concerning:

- Header information (filename, date, version, etc).
- Information about the component being scanned.
- Details of the measurement setup.
- Information on the probe (field, performance factor, etc).
- Data including the coordinate system used, frequencies or times and the data values.

Each section may be present, or not, and may include specific keywords allowing various parameters to be specified.

VI.6.2 XML format in IC-EMC

The file « scan_component_v6.xml» available in the subdirectory "examples\near_field" is used as an example in the following part. It contains the following information :

```
<?xml version="1.0" encoding="UTF-8"?>
<EmissionScan>
    <Component>
    </Component>
    <Setup>
    </Setup>
    <Probe>
    </Probe>
    <Data>
    </Data>
</EmissionScan>
```

Figure 6- 2 presents the results of the import of the XML file "scan_component_v6.xml". The file contains the measurement result of Hz field measured at 2.29 MHz above the surface of a microcontroller's package.

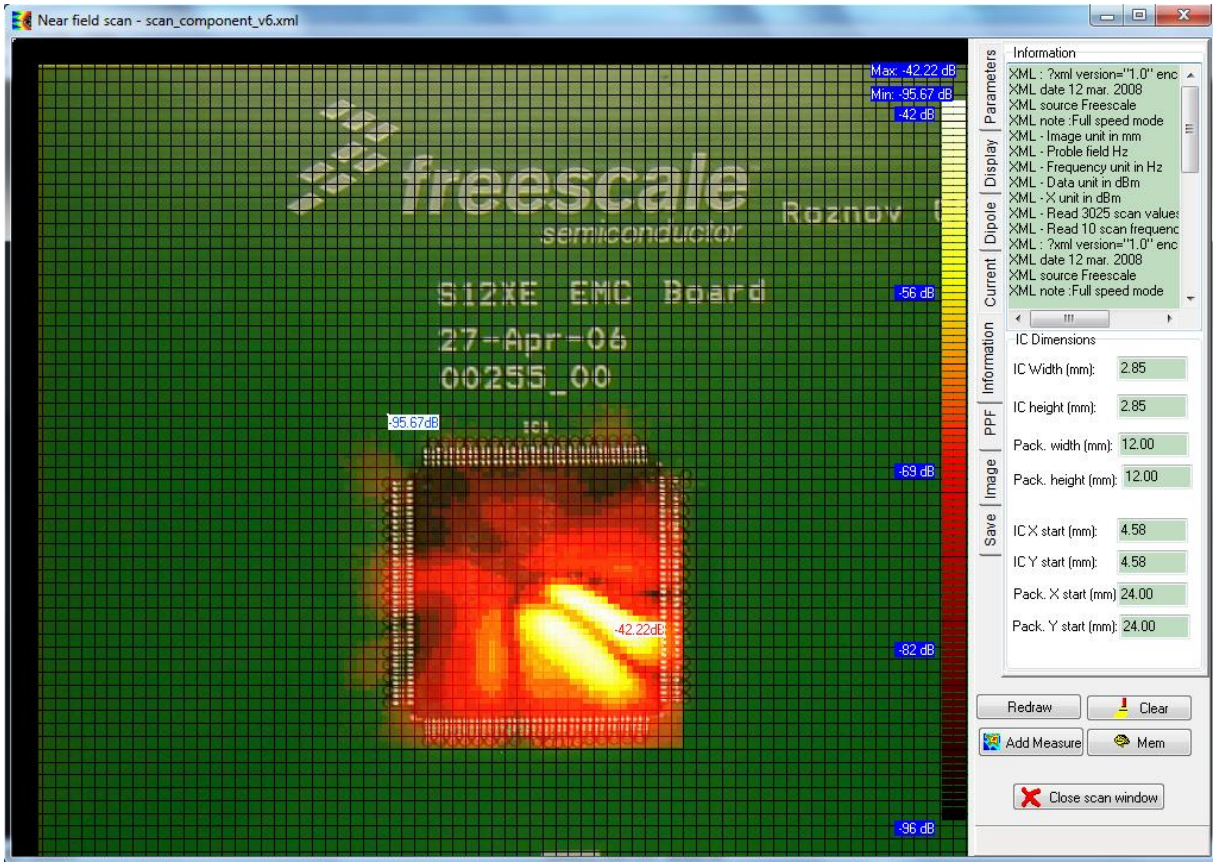


Figure 6- 2: The XML-based description of near-field scan data (examples\near_field\ scan_component_v6.xml)

When reading the XML file, the sub-item “Information” gives some indication about the data which has been decoded. We may see that IC-EMC loads several data files according to the main file request, through keyword <Data_files><Filename><Filename>..</Data_files>.

```
XML : ?xml version="1.0" encoding="UTF-8"?>
XML date 12 mar. 2008
XML source Freescale
```

```
XML note :Full speed mode
XML - Image unit in mm
XML - Proble field Hz
XML - Frequency unit in Hz
XML - Data unit in dBm
XML - X unit in dBm
XML - Read 3025 scan values
XML - Read 1 scan frequencies
```

VI.6.3 Remarks about the implementation of XML in IC-EMC

Keyword as defined in	Comments
<EmissionScan>	Opens the emission scan section
<Nfs_ver>	NFS template version; example 0.1
<Filename>	Document filename; example “scan_component.xml”
<File_ver>	Revision of the document file: example “1.0”
<Date>	The date of the file generation; example: 23 nov. 2007
<Source>	The XML data source; example “Freescale”
<Notes>	Notes added to the document
<Disclaimer>	Disclaimer information
<Copyright>	Copyright information
<Notes>	A notes section can be inserted anywhere in the file and the number of notes sections in the file is not limited.
<Component>	Opens the component section
<Component><Name>	Component name
<Component><Manufacturer>	Manufacturer description
<Component><Image>	Opens the Image subsection
<Component><Image><Path>	Link to the component image ; Example “component_image.JPG”
<Component><Image><Unit>	Image size unit; example “mm”
<Component><Image><Xsize>	Image size in X; example “81.0” (unit defined as mm)
<Component><Image><Ysize>	Image size in Y; example “82.0” (unit defined as mm)
<Component><Image><Xoffset>	Image shift in X
<Component><Image><Yoffset>	Image shift in Y
<Setup>	Opens the Setup section
<Setup><Config>	Opens the Configuration sub-section
<Setup><Config><Att>	Attenuation ; example: “0.0”
<Setup><Config><Average>	Average mode
<Setup><Config><Ref_level>	Reference level; example: “-10”; unit by default is dBm
<Setup><Config><Rbw>	Resolution Bandwidth; example: “3000.0” ; uniy by default is Hz
<Setup><Config><Vbw>	Video Bandwidth; example: “3000.0” ; uniy by default is Hz
<Setup><Config><Swp>	Sweep time; example: “0.143156653” ; unit by default is seconds
<Setup><Transducer>	Opens the Transducer sub-section. This section specifies information about cable losses and a preamplifier, if one is used during near-field scan.
<Setup><Transducer><Frequencies>	All information contained in this section concerns the frequencies at which the transducer gain data is listed.
<Setup><Transducer><Frequencies><Unit>	Specifies units of the frequencies at which the transducer gain data is listed.
<Setup><Transducer><Frequencies><List>	Specifies a list of frequencies at which the transducer gain is listed.
<Setup><Transducer><Gain>	Specifies a list of transducer gain values corresponding to the frequencies listed in the Frequencies sub-section of the Transducer section.
<Probe>	Opens the probe section
<Probe><Name>	Probe name; Example: “Freescale_Hz_1mm”
<Probe><Field >	Field measured with this probe; example: “HZ”
<Probe><Frequencies>	Opens the section that gives the list of frequencies available for each calibration point
<Probe><Frequencies><Unit>	Frequency unit of the probe calibration list
<Probe><Frequencies><List>	List of frequencies available for each calibration point; example

	“40E6 60E6 80E6 100E6 200E6 »
<Probe><Perf_factor>	Opens the probe performance factor section
<Probe><Perf_factor><Unit>	Unit of the probe performance factors
<Probe><Perf_factor><List>	List of probe performance factors according to frequency list; Example “-57.6 -54.5 -52.8 -50 -44 »
<Data>	Opens the data section
<Data><X0>	Absolute X coordinates of the scan
<Data><Y0>	Absolute Y coordinates of the scan
<Data><Z0>	Absolute Z coordinates of the scan
<Data><Xstep>	Added by B. Vrignon, E. Sicard to inform about the scan step in X axis
<Data><Ystep>	Added by B. Vrignon, E. Sicard to inform about the scan step in Y axis
<Data><Frequencies>	Opens the section that gives the list of frequencies available for each scan point
<Data><Frequencies><Unit>	Frequency unit
<Data><Frequencies><List>	Opens the frequency list; example (in Hz): 2290000.0 4580000.0 6870000.0 9160000.0 1.145E7 3.2E7 6.4E7 9.6E7 1.28E8 1.6E8
<Data><Times>	Specifies the Times section. All information contained in this section concerns the times at which the near-field scan data is measured.
<Data><Times><Unit>	Specifies units of the times at which the near-field scan data is listed.
<Data><Times><List>	Specifies a list of times at which the near-field scan measurement data is listed.
<Data><Measurement>	Opens the section that gives the measuring data
<Data><Measurement><Unit>	Measurement unit; example : “dBm”; default is dBm
<Data><Measurement><Unit_x>	Added to declare the X data unit.
<Data><Measurement><Unit_y>	Added to declare the Y data unit.
<Data><Measurement><Unit_z>	Added to declare the Z data unit.
<Data><Measurement><Data_files>	Specify the file path of data measurement
<Data><Measurement><List>	Opens the measurement list
26.0 29.0 2.0 -93.691 -93.726 -91.783 -90.772 -93.52 -91.865 -81.705 -78.408 -87.561 -92.142	X Y Z location in “unit_x”.. unit (Example mm); followed by measured data (Unit in this example: “dBm”) for each frequency defined in the Frequency list (here 10 values);

VI.6.4 Notes

1. The numbers use “.” Instead of “,”. Example: -64.38
2. The separation between numbers is the SPACE character instead of « , »

VI.6.5 Remarks about the hierarchy description

Recommendations have been proposed for a project architecture including several scan data (both emission and immunity), which gives some guidelines on how to store near-field scan files. Although beyond the scope of the XML standard which only focuses on basic keywords, these recommendations may eases the implementation of the standard. An example of how these files can be sorted in different folders has been proposed below:

```
+-- My Projects
|     +-- Project_name
|     |     |-- Project_name.xml
|     |
```

```
|     |     +-- EmissionScan
|     |     |     +-- Measurement 1
|     |     |     |     |-- Picture.jpg
|     |     |     |     |-- Dataxxx.xml
|     |     |     |     |-- Datayyy.xml
|     |     |     |     :
|     |     |     |
|     |     |     +-- Measurement n
|     |     |     |     :
|     |     :
|     |
|     +-- ImmunityScan
|     |     :
```

VI.7 Techno file .tec

The tool "ICEM Expert" builds simple CMOS digital IC emission model according to ICEM standard [ICEM] from basic technological information about the circuit. This type of analysis is particularly suited for evaluation of emission at pre-design stage or when an existing circuit is not available physically.

The construction of the model relies on technological information about CMOS process for several technological nodes contained in .TEC files. They are available in the subdirectory "lib\". The information provided in these files are not related to a particular foundry, since differences exist between the characteristics of CMOS processes provided by two different manufacturers. Moreover, one CMOS process provided by one manufacturer proposes various options (e.g. low power, general purpose, high-speed, high-performance, etc…). .TEC files provide information which is an average of CMOS process provided by different manufacturers. It corresponds to a kind of state-of-the-art of performances of a CMOS process node.

The following .TEC files are provided:

File	Description
Cmos06.tec	Technological information for 0.6 µm CMOS process
Cmos035.tec	Technological information for 0.35 µm CMOS process
Cmos025.tec	Technological information for 0.25 µm CMOS process
Cmos018.tec	Technological information for 0.18 µm CMOS process
Cmos012.tec	Technological information for 0.12 µm CMOS process
Cmos90n.tec	Technological information for 90 nm CMOS process
Cmos65n.tec	Technological information for 65 nm CMOS process
Cmos45n.tec	Technological information for 45 nm CMOS process
Cmos32n.tec	Technological information for 32 nm CMOS process
Cmos22n.tec	Technological information for 22 nm CMOS process
Default.tec	Default technological information, typical of a 65 nm CMOS process

Table 6- 1: Description of the symbol of the palette

All lines started by the symbol "*" are comment lines. A .TEC file may contain the following keywords:

Keywords	Description
VDD	Typical power supply voltage of core blocks
VIO	Typical power supply voltage of general-purpose CMOS buffer

TDelay	Typical delay in sec. of a CMOS gate
TCurrent	Typical current amplitude in Amps consumed by a CMOS gate
GActivity	Typical activity of the gates in the core blocks (from 0 to 1)
Cdecap	Typical decoupling capacitance in F associated to a CMOS gate
Csurf	Typical die intrinsic capacitance per surface (F/m²)
LDIL	Typical inductance per pin for a DIL package
LQFP	Typical inductance per pin for a QFP package
LBGA	Typical inductance per pin for a BGA package
LUBA	Typical inductance per pin for a µ-BGA package
LCSP	Typical inductance per pin for a CSP package
ML	Typical length of a CMOS transistor of an I/O buffer
MWN, MWP	Typical width of a NMOS and PMOS transistor of an I/O buffer

Table 6- 2: Keywords of .TEC file

VI.8 Library file .lib

.Lib file contains library of models of components such as MOSFET, BJT, diode, switch, temperature-dependent capacitance model, etc… The .Lib file is a text that can be created or edited by the user to add models of new component. As IC-EMC is compatible with WinSPICE and LTSPICE simulator, refer to the User's manual of these simulators to check the syntax of model's instance. A line starting with the symbol "*" is a a comment line.

Any schematic diagram that contains a MOSFET, a BJT, a diode, etc… requires the import of the library which contains the model of these components. The library can be imported by clicking on the menu command "Insert > Insert Library (.LIB)" or the button  . A command line starting with the keyword ".lib" is added on the schematic which provides the directory and the name of the library file.

A default library "spice.lib" is provided in IC-EMC in the subdirectory "\lib\". It contains the following models:

Model name	**Description**
DIOD	Basic model of a diode
CLAMP	Typical model of a ESD clamp diode
SCHOTTKY	Model of a power Schottky diode
CMODEL	Temperature dependence model of a capacitance
SWMOD	Basic model of a voltage-controlled switch
QMODN	Basic model of NPN BJT (modified Gummel-Poon model)
QMODP	Basic model of PNP BJT (modified Gummel-Poon model)
MN	Default model of a NMOS device for core block, Model Level 3
MP	Default model of a PMOS device for core block, Model Level 3
MN06	Typical model of a 0.6 µm NMOS device for core block, Model BSIM4
MP06	Typical model of a 0.6 µm PMOS device for core block, Model BSIM4
MN035	Typical model of a 0.35 µm NMOS device for core block, Model BSIM4
MP035	Typical model of a 0.35 µm PMOS device for core block, Model BSIM4
MN035HV	Typical model of a 0.35 µm NMOS device for I/O, Model Level 3

MP035HV	Typical model of a 0.35 µm PMOS device for I/O, Model Level 3
MN025	Typical model of a 0.25 µm NMOS device for core block, Model BSIM4
MP025	Typical model of a 0.25 µm PMOS device for core block, Model BSIM4
MN025HV	Typical model of a 0.25 µm NMOS device for I/O, Model Level 3
MP025HV	Typical model of a 0.25 µm PMOS device for I/O, Model Level 3
MN012	Typical model of a 0.12 µm NMOS device for core block, Model BSIM4
MP012	Typical model of a 0.12 µm PMOS device for core block, Model BSIM4
MN012HV	Typical model of a 0.12 µm NMOS device for I/O, Model BSIM4
MP012HV	Typical model of a 0.12 µm PMOS device for I/O, Model BSIM4
MN90N	Typical model of a 90 nm NMOS device for core block, Model BSIM4
MP90N	Typical model of a 90 nm PMOS device for core block, Model BSIM4
MN90NHV	Typical model of a 90 nm NMOS device for I/O, Model BSIM4
MP90NHV	Typical model of a 90 nm PMOS device for I/O, Model BSIM4
MN65N	Typical model of a 65 nm NMOS device for core block, Model BSIM4
MP65N	Typical model of a 65 nm PMOS device for core block, Model BSIM4
MN65NHV	Typical model of a 65 nm NMOS device for I/O, Model BSIM4
MP65NHV	Typical model of a 65 nm PMOS device for I/O, Model BSIM4
MN45N	Typical model of a 45 nm NMOS device for core block, Model BSIM4
MP45N	Typical model of a 45 nm PMOS device for core block, Model BSIM4
MN45NHV	Typical model of a 45 nm NMOS device for I/O, Model BSIM4
MP45NHV	Typical model of a 55 nm PMOS device for I/O, Model BSIM4
MN32N	Typical model of a 32 nm NMOS device for core block, Model BSIM4
MP32N	Typical model of a 32 nm PMOS device for core block, Model BSIM4
MN32NHV	Typical model of a 32 nm NMOS device for I/O, Model BSIM4
MP32NHV	Typical model of a 32 nm PMOS device for I/O, Model BSIM4

Table 6- 3: List of component's models available in the default library "\lib\spice.lib"

References

[TOU02]	“Touchstone® File Format Specification – Revision 1.1”, EIA/IBIS Open Forum, 2002.
[She09]	J. Shepherd, A. Nakamura, F. Lafon, E. Sicard, M. Ramdani, D. Pommerenke, G. Muchaidze, S. Serpaud "Developing a Universal Exchange Format for Near-Field Scan Data", oral presentation at IEEE EMC Symposium Austin, Texas, USA, 2009.